User's Manual

ASSP

R-IN32M3 Series User's Manual

- R-IN32M3-CL

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Document number: R18UZ0005EJ0202
Issue date : Dec 25, 2014

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Instructions for the use of product

In this section, the precautions are described for over whole of CMOS device.
Please refer to this manual about individual precaution.
When there is a mention unlike the text of this manual, a mention of the text takes first priority

1.Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

-The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2.Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

-The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3.Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

-The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4.Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

-When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

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・Real-Time OS　Accelerator and Hardware Real-Time OS is based on Hardware Real-Time OS of “ARTESSO” made in KERNELON SILICON Inc.

How to use this manual

1. Purpose and target readers

This manual is intended for users who wish to understand the functions of Industrial Ethernet network LSI "R-IN32M3-CL" (µPD60510F1-HN4-A) for designing application of it.

It is assumed that the reader of this manual has general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

Literature — Literature may be preliminary versions. Note, however, that the following descriptions do not indicate "Preliminary". Some documents on cores were created when they were planned or still under development. So, they may be directed to specific customers. Last four digits of document number(described as ****) indicate version information of each document. Please download the latest document from our web site and refer to it.

The document related to R-IN32M3-CL

Document name	Document number
R-IN32M3 series Datasheet	R18DS0008EJ****
R-IN32M3-EC User's Manual	R18UZ0003EJ****
R-IN32M3series User's Manual Peripheral function	R18UZ0007EJ****
R-IN32M3 Series Proguraming Manual (OS edition)	R18UZ0011EJ****
R-IN32M3 Series Proguraming Manual (Driver edition)	R18UZ0009EJ****
R-IN32M3-CL User's Manual	This manual

2. Notation of Numbers and Symbols

Weight in data notation: Left is high-order column, right is low-order column

Active low notation:

xxxZ (capital letter Z after pin name or signal name)

or xxx_N (capital letter _N after pin name or signal name)

or xxnx (pin name or signal name contains small letter n)

Note:

explanation of (Note) in the text

Caution:

Item deserving extra attention

Remark:

Supplementary explanation to the text

Numeric notation:

Binary ⋯ xxxx , xxxxB or n'bxxxx (n bits)

Decimal ⋯ xxxx

Hexadecimal ⋯ xxxxH or n'hxxxx (n bits)

Prefixes representing powers of 2 (address space, memory capacity):

K (kilo)⋯ $2^{10} = 1024$

M (mega)⋯ $2^{20} = 1024^2$

G (giga)⋯ $2^{30} = 1024^3$

Data Type:

Word ⋯ 32 bits

Halfword ⋯ 16 bits

Byte ⋯ 8 bits

Contents

1. Overview 1

1.1 Introduction 1
1.2 Overview 2
1.3 INTERNAL BLOCK DIAGRAM 4
1.4 Pin Placement (Top View) 5

2. Signals by function 6

2.1 Signals by function 6
2.1.1 Ethernet Signals 6
2.1.2 External Memory Interface Signals 8
2.1.3 External MCU Interface Signals 9
2.1.4 Port Signal, Real-time port Signals 10
2.1.5 Serial Flash ROM Interface Signals 14
2.1.6 DMA Interface Signals 14
2.1.7 External Interrupt Input Signals 15
2.1.8 Timer I/O Signals 15
2.1.9 Watchdog Timer Output Signal 15
2.1.10 Trace Signals 16
2.1.11 CPU Power Control Signal 16
2.1.12 Serial Interface Signals 16
2.1.13 CC-Link IE Field Signals (Intelligent device station) 17
2.1.14 CC-Link Signals (Intelligent device station) 18
2.1.15 CC-Link Signals (Remote device station) 19
2.1.16 System Signals 20
2.1.17 Test Signals 21
2.1.18 Operation mode Setting Signals 21
2.2 Port status 22
2.3 Operation mode monitor functions 23
2.4 Buffer function conversion function 23
2.5 Buffer Types and Recommended Connections for Unused Pins 24
2.5.1 Ethernet Signals 24
2.5.2 External Memory/ MCU Interface Signals 25
2.5.3 System Signals 25
2.5.4 Test Signals 26
2.5.5 Port Signals 27

2.5.6 Operation Mode Setting Signals 28
2.5.7 CC-Link IE Field Signal (Intelligent device station) 28
2.5.8 CC-Link Signal (Intelligent device station, Remote device station) 28
2.5.9 Trace Signals 28

3. Memory Maps 29

4. Exception handling function 33

4.1 Exceptions list 33
4.2 Interrupt list 34

5. Peripheral function 38

6. CC-Link IE Field (Intelligent device station) Function 39

6.1 CC-Link IE Field (Intelligent device station) control register 39
6.1.1 CC-Link IE Field (Intelligent device station) clock gate register（CIECLKGTD） 40
6.1.2 CC-Link IE Field (Intelligent device station) wait delay register（CIEWAITDLY） 41
6.1.3 CC-Link IE Field (Intelligent device station) bus size control register (CIEBSC) 42
6.1.4 CC-Link IE Field (Intelligent device station) bus bridge control register (CIESMC) 42

7. Port function 43

7.1 Features 43
7.2 Port configuration 44
7.3 Registers 46
7.3.1 Port registers (P, RP) 52
7.3.2 Port mode registers (PM, RPM) 55
7.3.3 Port mode control register (PMC, RPMC) 58
7.3.4 Port function control registers (PFC, RPFC) 61
7.3.5 Port function control expansion registers (PFCE, RPFCE) 64
7.3.6 Port pin input registers (PIN, RPIN) 67
7.4 Available combinations of alternate functions 70
7.5 Buffer function change registers (DRCTLP) 74
7.5.1 Port 0 buffer function change registers (DRCTLP0L, DRCTLP0H) 75
7.5.2 Port 1 Buffer function change register (DRCTLP1L, DRCTLP1H) 76
7.5.3 Port 2 Buffer function change register (DRCTLP2L, DRCTLP2H) 77
7.5.4 Port 3 Buffer function change register (DRCTLP3L, DRCTLP3H) 78
7.5.5 Port 4 Buffer function change register (DRCTLP4L, DRCTLP4H) 79
7.5.6 Port 5 Buffer function change register (DRCTLP5L, DRCTLP5H) 80
7.5.7 Port 6 Buffer function change register (DRCTLP6L, DRCTLP6H) 81

7.5.8 Port 7 Buffer function change register (DRCTLP7L, DRCTLP7H) 82
7.5.9 Real-time port 0 Buffer function change register (DRCTLRP0L, DRCTLRP0H) 83
7.5.10 Real-time port 1 buffer function change registers (DRCTLRP1L, DRCTLRP1H) 84
7.5.11 Real-time port 2 Buffer function change register (DRCTLRP2L, DRCTLRP2H) 85
7.5.12 Real-time port 3 Buffer function change register (DRCTLRP3L, DRCTLRP3H) 86
7.6 Operation of port functions 87
7.6.1 Reading and writing via I/O ports 87
7.6.2 Alternate function pin output status in control mode 87
7.7 Trigger-synchronous ports (RP00 to RP37) 88

8. Electrical Specifications 89

Contents of figures

Figure 3.1 Memory map (ALL) 29
Figure 3.2 Memory map (APB Peripheral registers area) 30
Figure 3.3 Memory map (External memory area) 31
Figure 3.4 Memory map (CC-Link Master area) 31
Figure 3.5 External MCU interface area 32
Figure 6.1 Data sampling timing example 41
Figure 7.1 Basic port circuit configuration 45
Figure 7.2 Port registers (in 8-bit notation) 52
Figure 7.3 Port registers (in 16-bit notation) 53
Figure 7.4 Port registers (in 32-bit notation) 54
Figure 7.5 Port mode registers (in 8-bit notation) 55
Figure 7.6 Port mode registers (in 16-bit notation) 56
Figure 7.7 Port mode registers (in 32-bit notation) 57
Figure 7.8 Port mode control registers (in 8-bit notation) 58
Figure 7.9 Port mode control registers (in 16-bit notation) 59
Figure 7.10 Port mode control registers (in 32-bit notation) 60
Figure 7.11 Port function control registers (in 8-bit notation) 61
Figure 7.12 Port function control registers (in 16-bit notation) 62
Figure 7.13 Port function control expansion registers (in 8-bit notation) 64
Figure 7.14 Port function control expansion registers (in 16-bit notation) 65
Figure 7.15 Port function control expansion registers (in 32-bit notation) 66
Figure 7.16 Port pin input registers (in 8-bit notation) 67
Figure 7.17 Port pin input registers (in 16-bit notation) 68
Figure 7.18 Configuration of Trigger-Synchronous Ports 88

Contents of tables

Table2.1 Operation mode setting signals that can be confirmed 23
Table4.1 Interrupt list 34
Table 6.1 CC-Link IE Field outline specifications..... 39
Table 6.2 CC-Link IE Field (Intelligent device station) control registers overview 39

1. Overview

1.1 Introduction

Ethernet communication continues to spread rapidly in the field of industrial automation as manufacturers seek to improve the capability, efficiency, and flexibility of their organizations. Modern Industrial Ethernet applications require high-speed real-time response, low power consumption, and high performance. These requirements are not necessarily met by traditional methods such as hard-wired Ethernet processors or dedicated high-speed CPUs.

Renesas' R-IN32M3-CL of large-scale integrated circuits (LSI) are specifically tailored to meet the demands of Industrial Ethernet applications. Key features include:

- High-speed, real-time, deterministic, low-latency, low-jitter response for real-time applications
- Low power consumption
- Integrated ARM Cortex-M3 core for flexibility
- Integrated Real-Time OS Accelerator with support for µITRON version 4.0
- Integrated Gigabit Ethernet MAC
- Dedicated, DMA controller and buffer for the network processor
- High performance with low CPU usage by offloading functions to Real-Time OS Accelerator
- Multiple timers, serial interfaces, general purpose I/O (GPIO), external memory interfaces

1.2 Overview

Table1.1 Overview of R-IN32M3-CL(1/2)

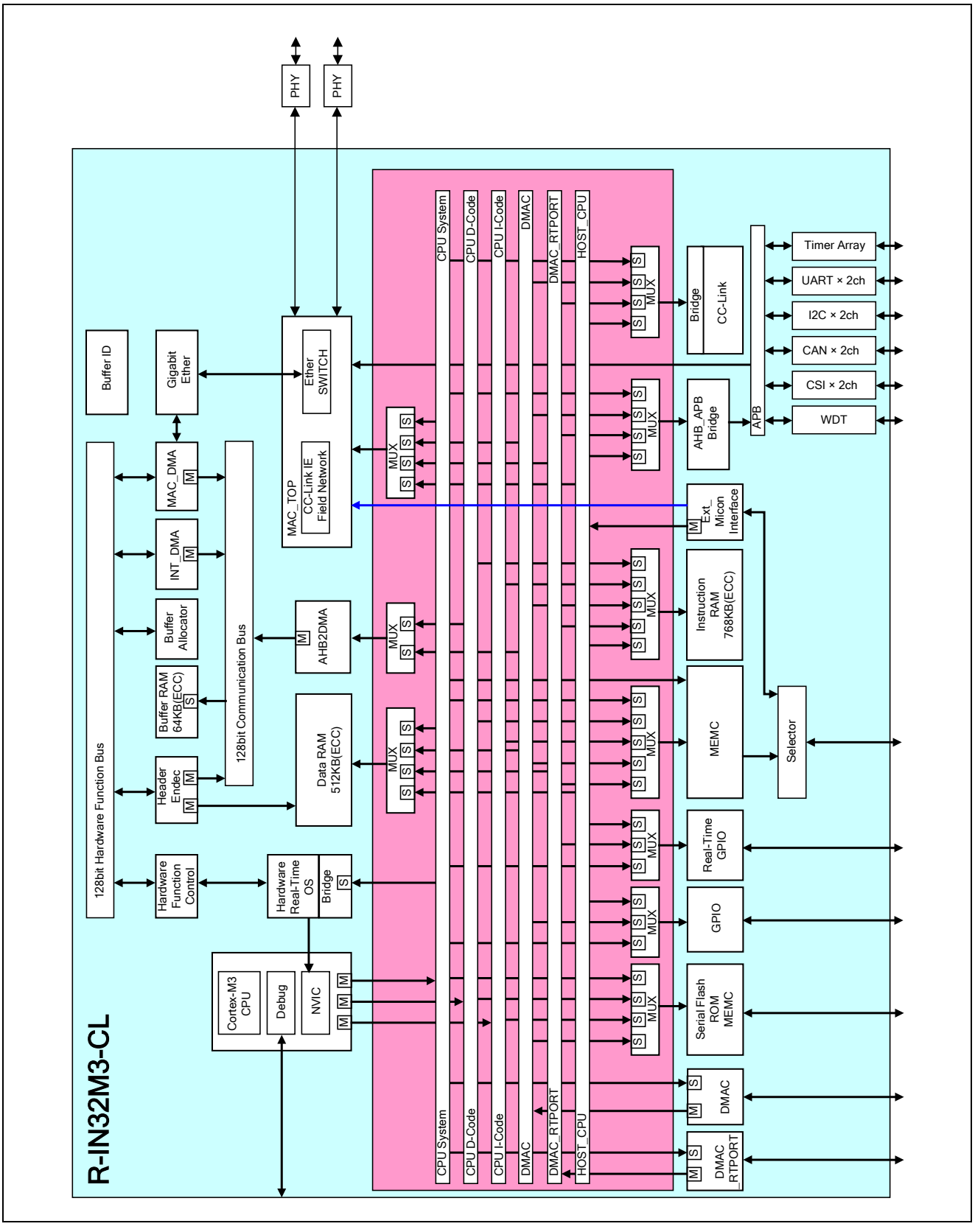
Item \ Product	R-IN32M3-CL
CPU cores	ARM Cortex-M3 32-bit RISC CPU + Real-Time OS Accelerator (Hardware Real-Time OS, HW-RTOS)
Operating frequency	100MHz
Instruction set	Thumb®-2 instruction ARMv7-M architecture
Instruction RAM	768KByte (RAM w/ECC)
Data RAM	512KByte (RAM w/ECC)
Buffer RAM	64KByte (RAM w/ECC)
Internal System Bus	- 32-bit system bus at 100MHz - 128-bit communication bus at 100MHz
DMA Bus (System Bus Side)	- 4 channels + 1 channel (for Real-time port) - Supports software and various interrupt-triggered DMA
Boot options	- Serial Flash ROM Boot - External Memory Boot - External MCU Boot
External Memory Support	- 16-bit or 32-bit bus interface - Page ROM / ROM / SRAM interface - Synchronous burst memory interface - Four chip selects for external SRAM - 256MByte (max) external memory space - Programmable wait function
External MCU interface	- 16-bit or 32-bit bus interface - General-purpose interface for static memory - Address space:2MByte (Instruction RAM, Data RAM, Register area)
Serial Flash ROM Memory Controller	- Support serial interface compatible with SPI of the companies - Support direct boot from serial memory device - Support Fast Read, Fast Read Dual Output, Fast Read Dual I/O mode - Direct layout in memory space
Interrupt	- 29 external interrupt ports
Internal Peripheral Circuit	
I/O Ports	CMOS I/O:96ports(max)
System Timers	- Internal timer of Hardware RTOS
	- internal timer of CPU
	- 4channel timer array - 32bit counter & 32bit data register - counter by external signal

Table1.1 Overview of R-IN32M3-CL(2/2)

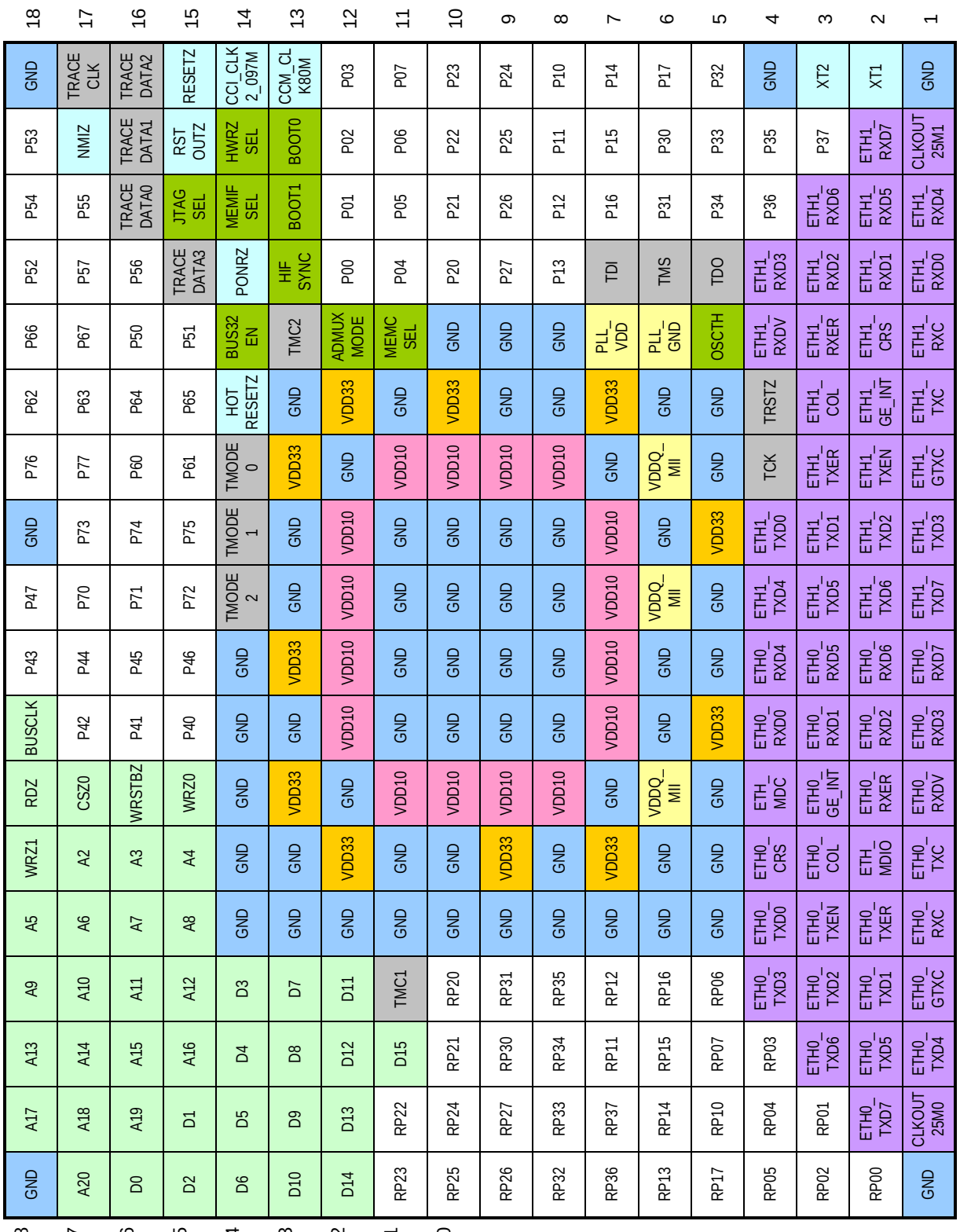
Item \ Product	R-IN32M3-CL
Internal Peripheral Circuit	
Watchdog Timer	- 1 channel - Software-triggered start mode - Watchdog error response options: - Generate Non-Maskable Interrupt (NMI) - Generate Reset
Asynchronous serial interface	- 2 channels - Full duplex - FIFOs: 10-bit x 16 receive and 8-bit x 16 transmit - Support output of receive errors and status - Character length: 7 or 8-bit - Parity bit options: odd, even, 0- , none - Transmit stop bits: 1 or 2-bit
I2C Serial interface	- 2 channels - Operation modes: normal or high-speed - Transfer modes: single-transfer mode, or continuous-transfer mode - Transmission data length: 8-bit
CAN controller	- 2 channels - Conforming to ISO11898 - Support to transfer and receive normal frame and expand frame - Transmission speed: 1Mbps (max)
Clock Synchronized Serial Interface	- 2 channels - Synchronized Serial data transmission by three-wire system - Selectable Master mode or Slave mode - Built-in Baud-rate generator - Transmission data length: 7bit - 16bit
CC-Link	- Intelligent device station Note3 <R> - Remote device station
10/100/1000Mbps Ether MAC Note1	- 1 channel - Built-in 2-port switch - GMII / MII interface
CC-Link IE	CC-Link IE Field (Intelligent device station)
On-chip debug function	- Select serial wire or JTAG - Support Full Trace(Built-in ETM)
Internal PLL	Generates various clocks from 25MHz input clock
Power supply voltage	I/O:VDD33 = 3.3±0.3V Internal circuit :VDD10 = 1.0±0.1V

Note. Please ask us about a detail for support.

1.3 INTERNAL BLOCK DIAGRAM



1.4 Pin Placement (Top View)



	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	
18	GND	A17	A13	A9	A5	WRZ1	RDZ	BUSCLK	P43	P47	GND	P76	P62	P66	P52	P54	P53	GND	18
17	A20	A18	A14	A10	A6	A2	CS20	P42	P44	P70	P73	P77	P63	P67	P57	P55	NMIZ	TRACE CLK	17
16	D0	A19	A15	A11	A7	A3	WRSTBZ	P41	P45	P71	P74	P60	P64	P50	P56	TRACE DATA0	TRACE DATA1	TRACE DATA2	16
15	D2	D1	A16	A12	A8	A4	WR20	P40	P46	P72	P75	P61	P65	P51	TRACE DATA3	JTAG SEL	RST OUTZ	RESETZ	15
14	D6	D5	D4	D3	GND	GND	GND	GND	GND	TMODE 2	TMODE 1	TMODE 0	HOT RESETZ	BUS32 EN	PONRZ	MEMIF SEL	HWRZ SEL	CCI_CLK 2_097M	14
13	D10	D9	D8	D7	GND	GND	VDD33	GND	VDD33	GND	GND	VDD33	GND	TMC2	HIF SYNC	BOOT1	BOOT0	CCM_CLK 80M	13
12	D14	D13	D12	D11	GND	VDD33	GND	VDD10	VDD10	VDD10	VDD10	GND	VDD33	ADMUX MODE	P00	P01	P02	P03	12
11	RP23	RP22	D15	TMC1	GND	GND	VDD10	GND	GND	GND	GND	VDD10	GND	MEMC SEL	P04	P05	P06	P07	11
10	RP25	RP24	RP21	RP20	GND	GND	VDD10	GND	GND	GND	GND	VDD10	VDD33	GND	P20	P21	P22	P23	10
9	RP26	RP27	RP30	RP31	GND	VDD33	VDD10	GND	GND	GND	GND	VDD10	GND	GND	P27	P26	P25	P24	9
8	RP32	RP33	RP34	RP35	GND	GND	VDD10	GND	GND	GND	GND	VDD10	GND	GND	P13	P12	P11	P10	8
7	RP36	RP37	RP11	RP12	GND	VDD33	GND	VDD10	VDD10	VDD10	VDD10	GND	VDD33	PLL_VDD	TDI	P16	P15	P14	7
6	RP13	RP14	RP15	RP16	GND	GND	VDDQ_MII	GND	GND	VDDQ_MII	GND	VDDQ_MII	GND	PLL_GND	TMS	P31	P30	P17	6
5	RP17	RP10	RP07	RP06	GND	GND	GND	VDD33	GND	GND	VDD33	GND	GND	OSCTH	TDO	P34	P33	P32	5
4	RP05	RP04	RP03	ETH0_TXD3	ETH0_TXD0	ETH0_CRS	ETH_MDC	ETH0_RXD0	ETH0_RXD4	ETH1_TXD4	ETH1_TXD0	TCK	TRSTZ	ETH1_RXDV	ETH1_RXD3	P36	P35	GND	4
3	RP02	RP01	ETH0_TXD6	ETH0_TXD2	ETH0_TXEN	ETH0_COL	ETH0_GE_INT	ETH0_RXD1	ETH0_RXD5	ETH1_TXD5	ETH1_TXD1	ETH1_TXER	ETH1_COL	ETH1_RXER	ETH1_RXD2	ETH1_RXD6	P37	XT2	3
2	RP00	ETH0_TXD7	ETH0_TXD5	ETH0_TXD1	ETH0_TXER	ETH_MDIO	ETH0_RXER	ETH0_RXD2	ETH0_RXD6	ETH1_TXD6	ETH1_TXD2	ETH1_TXEN	ETH1_GE_INT	ETH1_CRS	ETH1_RXD1	ETH1_RXD5	ETH1_RXD7	XT1	2
1	GND	CLKOUT 25M0	ETH0_TXD4	ETH0_GTXC	ETH0_RXC	ETH0_TXC	ETH0_RXDV	ETH0_RXD3	ETH0_RXD7	ETH1_TXD7	ETH1_TXD3	ETH1_GTXC	ETH1_TXC	ETH1_RXC	ETH1_RXD0	ETH1_RXD4	CLKOUT 25M1	GND	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	

2. Signals by function

2.1 Signals by function

2.1.1 Ethernet Signals

(1) PHY Interface

Pin Name	I/O	Function	Active	Level during reset & Level after reset
ETH0_TXC	I	Ethernet 0 10M/100M Transmit clock port (2.5MHz/25MHz)	↑	-
ETH0_GTXC	O	Ethernet 0 1G Transmit clock port (125MHz)	↑	-Note
ETH0_TXEN	O	Ethernet 0 Transmit enable port	High	Low
ETH0_TXER	O	Ethernet 0 Transmit error port	High	Low
ETH0_TXD0-ETH0_TXD7	O	Ethernet 0 Transmit data port	-	Low
ETH0_GE_INT	I	Ethernet 0 PHY interrupt port	High/Low	-
ETH0_RXC	I	Ethernet 0 Receive clock port	↑	-
ETH0_RXDV	I	Ethernet 0 Receive enable port	High	-
ETH0_RXER	I	Ethernet 0 Receive error port	High	-
ETH0_RXD0-ETH0_RXD7	I	Ethernet 0 Receive data port	-	-
ETH0_CRS	I	Ethernet 0 Carrier sense port	High	-
ETH0_COL	I	Ethernet 0 Collision port	High	-
ETH1_TXC	I	Ethernet 1 10M/100M Transmit clock port (2.5MHz/25MHz)	↑	-
ETH1_GTXC	O	Ethernet 1 1G Transmit clock port (125MHz)	↑	-Note
ETH1_TXEN	O	Ethernet 1 Transmit enable port	High	Low
ETH1_TXER	O	Ethernet 1 Transmit error port	High	Low
ETH1_TXD0-ETH1_TXD7	O	Ethernet 1 Transmit data port	-	Low
ETH1_GE_INT	I	Ethernet 1 PHY interrupt port	High/Low	-
ETH1_RXC	I	Ethernet 1 Receive clock port	↑	-
ETH1_RXDV	I	Ethernet 1 Receive enable port	High	-
ETH1_RXER	I	Ethernet 1 Receive error port	High	-
ETH1_RXD0-ETH1_RXD7	I	Ethernet 1 Receive data port	-	-
ETH1_CRS	I	Ethernet 1 Carrier sense port	High	-
ETH1_COL	I	Ethernet 1 Collision port	High	-
ETH_MDC	O	Ethernet Serial management interface clock	↑	Low
ETH_MDIO	I/O	Ethernet Serial management interface data input/output	-	Hi-Z

Note. Out put the 125MHz clock.

(2) Other Signals

Pin Name	I/O	Function	Shared Port	Active	Level during reset & Level after reset
PHYLINK0, PHYLINK1	I	PHY Link port (for EtherSwitch)	P06-P07	High	Hi-Z With internal pull-up resistor
ETHSWSECOUT	O	EtherSwitch Event par 1sec output port	P24	High	

2.1.2 External Memory Interface Signals

Pin Name	I/O	Function	Shared Signal	Shared port	Active	Level during reset	Level after reset
BUSCLK	O	Bus clock output port	-	-	-	-	
CSZ0	O	Chip select signal output port	HCSZ	-	Low	Hi-Z With internal pull-up resistor	
CSZ1	O		HPGCSZ	P44			
CSZ2	O		-	P51			
CSZ3	O		-	P50			
A1	O	Address output port	HA1	P40	-	Hi-Z With internal pull-up resistor	Low
A2-A20	O		HA2-HA20	-		Hi-Z With internal pull-down resistor	
A21-A27	O		-	RP21-RP27			Hi-Z With internal pull-down resistor
D0-D15[Note1]	I/O	Data bus port	HD0-HD15	-			
D16-D31 [Note1]	I/O		HD16-HD31	RP30-RP37 RP10-RP17	-	Hi-Z With internal pull-up resistor	
RDZ	O	Read strobe output port	HRDZ	-	Low	Hi-Z With internal pull-up resistor	High
WRSTBZ	O	Write strobe output port	HWRSTBZ	-	Low		
WRZ0, WRZ1/ BENZ0, BENZ1	O	Effectively Byte lane strobe output port	HWRZ0, HWRZ1/ HBENZ0, HBENZ1	-	Low		
WRZ2, WRZ3/ BENZ2, BENZ3	O		HWRZ2, HWRZ3/ HBENZ2, HBENZ3	RP06, RP07			
WAITZ	I	Wait signal input port	HWAITZ	P41	Low	Hi-Z With internal pull-up resistor	
WAITZ1-WAITZ3 Note2			-	P45-P47			
BCYSTZ / ADVZ Note3	O	Address valid output port	HBCYSTZ	RP20	Low	Hi-Z With internal pull-up resistor	

Remark External Memory Interface Signal expects BUSCLK is an input signal while the internal reset signal (HRESETZ) is active.

Note1. When using synchronous burst access MEMC this port is shared with Address port when ADMUXMODE is high.

2. This port is available only when using synchronous burst access MEMC.

3. This port functions as BCYSTZ when using asynchronous SRAM MEMC, it functions as ADVZ when using synchronous burst access MEMC

2.1.3 External MCU Interface Signals

Pin Name	I/O	Function	Shared Signal	Shared port	Active	Level during reset & Level after reset
HBUSCLK	I	Bus clock for Host MCU output port	INTPZ11	P43	-	Hi-Z With internal pull-up resistor
HCSZ	I	Chip select signal input port	CSZ0	-	Low	
HPGCSZ	I	Pogrom mode Chip select signal input port	CSZ1	P44	Low	
HWAITZ	O	Wait signal output port	WAITZ	P41	Low	
HA1	I	Address input port	A1	P40	-	Hi-Z With internal pull-up resistor
HA2-HA20	I		A2-A20	-		Hi-Z With internal pull-down resistor
HD0-HD15	I/O	Data bus port	D0-D15	-	-	
HD16-HD31	I/O		D16-D31	RP30-RP37 RP10-RP17		Hi-Z With internal pull-up resistor
HRDZ	I	Read strobe input port	RDZ	-	Low	Hi-Z With internal pull-up resistor
HWRSTBZ	I	Write strobe output port	WRSTBZ	-	Low	
HWRZ0, HWRZ1/ HBENZ0,HBENZ1	I	Effectively Byte lane strobe input port	WRZ0, WRZ1/ BENZ0, BENZ1	-	Low	
HWRZ2, HWRZ3/ HBENZ2,HBENZ3	I		WRZ2, WRZ3/ BENZ2, BENZ3	RP06, RP07		
HERROUTZ	O	Error interrupt output port	SLEEPING	P42	Low	High
HBCYSTZ	I	Bus cycle input port	BCYSTZ / ADVZ	RP20	Low	Hi-Z With internal pull-up resistor

Caution When you use asynchronous mode, please input Low into a HBUSCLK pin..

Remark External MCU interface signals operate as an External MCU interface durinug reset.

2.1.4 Port Signal, Real-time port Signals

Port Signals and Real-time port Signals are configured as 12 sets of 8-bit ports.

They are able to realize 32-bit access by grouping 4 ports; i.e. Ports 0-3, Ports 4-7 or Real-time ports 0-3.

(1/4)

	Port Name	Mode 1	Mode 2	Mode 3	Mode 4	Level during reset & Level after reset
P0	P00	INTPZ0	-	CCI_RUNLEDZ	-	Hi-Z With internal pull-up resistor
	P01	INTPZ1	-	-	-	
	P02	INTPZ2	-	CCI_DLINKLEDZ	-	
	P03	INTPZ3	-	CCI_ERRLEDZ	CCS_MON5	
	P04	INTPZ4	-	CCI_LERR1LEDZ	CCS_MON6	
	P05	INTPZ5	-	CCI_LERR2LEDZ	CCS_MON7	
	P06	PHYLINK0	-	CCI_SDLEDZ	CCS_MON0	
	P07	PHYLINK1	-	CCI_RDLEDZ	CCS_RESOUT	
P1	P10	-	-	-	CCS_REFSTB	Hi-Z With internal pull-up resistor
	P11	-	-	-	CCS_MON4	Hi-Z With internal pull-down resistor
	P12	INTPZ6	-	CCI_NMIZ	-	Hi-Z With internal pull-up resistor
	P13	INTPZ7	-	CCI_WDTIZ / CCS_WDTZ / CCM_WDTENZ	-	
	P14	SMSCK	-	-	-	
	P15	SMSI	-	-	-	
	P16	SMSO	-	-	-	
	P17	SMCSZ	-	-	-	
P2	P20	RXD0	−	CCM_LINKERRZ	-	Hi-Z With internal pull-up resistor
	P21	TXD0	−	CCM_ERRZ	-	
	P22	INTPZ8	-	CCS_IOTENSU	-	
	P23	INTPZ9	-	CCS_SENYU0	-	
	P24	INTPZ10	ETHSWSECOUT	CCS_SENYU1	-	
	P25	WDTOUTZ	−	CCS_ERRZ	-	
	P26	TIN1	TOUT1	CCM_RUNZ / CCS_RUNZ	-	
	P27	TIN0	TOUT0	-	-	

(2/4)

	Port Name	Mode 1	Mode 2	Mode 3	Mode 4	Level during reset & Level after reset
P3	P30	RXD1	-	-	-	Hi-Z With internal pull-up resistor
	P31	TXD1	-	-	-	
	P32	DMAREQZ1	-	-	CCS_MON1	
	P33	DMAACKZ1	CCI_ WAITEDGEH	-	CCS_MON2	
	P34	DMATCZ1	CCI_WRLENH	-	CCS_MON3	
	P35	CSISCK1	INTPZ22	CCM_IRZ	-	
	P36	CSISI1	INTPZ23	CCS_FUSEZ	-	
	P37	CSISO1	INTPZ24	CCM_MSTZ	-	
P4	P40	A1	HA1	-	-	Hi-Z 内蔵 Pull-up 抵抗により ハイ・レベル
	P41	WAITZ	HWAITZ	-	-	
	P42	SLEEPING	HERROUTZ	CCM_SDGCZ	-	
	P43	INTPZ11	HBUSCLK	-	-	
	P44	CSZ1	HPGCSZ	-	-	
	P45	CSISCK0	WAITZ1	-	-	
	P46	CSISI0	WAITZ2	-	-	
	P47	CSISO0	WAITZ3	-	-	
P5	P50	CSZ3	-	CCM_LNKRUNZ / CCS_LNKRUNZ	-	
	P51	CSZ2	-	CCM_RDLEDZ / CCS_RDLEDZ	-	
	P52	TIN3	TOUT3	CCS_SDGATEON	-	Hi-Z With internal pull-down resistor
	P53	CRXD0	CCS_RD	CCM_RD	-	Hi-Z With internal pull-up resistor
	P54	CTXD0	CCS_SD	CCM_SD	-	
	P55	CRXD1	-	-	-	
	P56	CTXD1	-	CCI_PHYREZ1	-	
	P57	TIN2	TOUT2	CCI_PHYREZ0	-	

(3/4)

	Port Name	Mode 1	Mode 2	Mode 3	Mode 4	Level during reset & Level after reset
P6	P60	SCL0	−	−	−	Hi-Z With internal pull-up resistor
	P61	SDA0	−	−	−	
	P62	RTDMAREQZ	−	CCM_MDIN0	−	
	P63	RTDMAACKZ	−	CCM_MDIN1	−	
	P64	RTDMATCZ	−	CCM_MDIN2	−	
	P65	DMAREQZ0	−	CCM_MDIN3	−	
	P66	DMAACKZ0	−	CCI_INTZ	−	
	P67	DMATCZ0	−	−	−	
P7	P70	CSICS00	-	CCS_STATION_NO_0 / CCM_SNIN0	−	
	P71	CSICS01	-	CCS_STATION_NO_1 / CCM_SNIN1	−	
	P72	CSICS10	-	CCS_STATION_NO_2 / CCM_SNIN2	−	
	P73	CSICS11	-	CCS_STATION_NO_3 / CCM_SNIN3	−	
	P74	INTPZ12	-	CCS_STATION_NO_4 / CCM_SNIN4	−	
	P75	INTPZ13	-	CCS_STATION_NO_5 / CCM_SNIN5	−	
	P76	INTPZ14	-	CCS_STATION_NO_6 / CCM_SNIN6	−	
	P77	INTPZ15	-	CCS_STATION_NO_7 / CCM_SNIN7	−	

RP0x-RP3x are Real-time ports which can transfer data via a dedicated DMA comtroller, and are unaffected by bus congestion. They are able to perform input and output of the port by 32 bit unit in sync with DMA transfer trigger by DMA Controller for exclusive use of the Real-time port.

(4/4)

	Port Name	Mode 1	Mode 2	Mode 3	Mode 4	Level during reset & Level after reset
RP0	RP00	INTPZ16	SCL1	CCM_SDLEDZ / CCS_SDLEDZ	−	Hi-Z With internal pull-up resistor
	RP01	INTPZ17	SDA1	CCM_SMSTZ	−	
	RP02	INTPZ18	-	CCS_BS1	−	
	RP03	INTPZ19	-	CCS_BS2	−	
	RP04	INTPZ20	-	CCS_BS4	−	
	RP05	INTPZ21	−	CCS_BS8	−	
	RP06	WRZ2/BENZ2	HWRZ2/HBENZ2	-	−	
	RP07	WRZ3/BENZ3	HWRZ3/HBENZ3	−	−	
RP1	RP10	D24/HD24	−	−	−	Hi-Z With internal pull-up resistor
	RP11	D25/HD25	−	−	−	
	RP12	D26/HD26	−	−	−	
	RP13	D27/HD27	−	−	−	
	RP14	D28/HD28	−	−	−	
	RP15	D29/HD29	−	−	−	
	RP16	D30/HD30	−	−	−	
	RP17	D31/HD31	−	−	−	
RP2	RP20	BCYSTZ / ADVZ	HBCYSTZ	−	−	Hi-Z With internal pull-up resistor
	RP21	A21	−	−	−	Hi-Z With internal pull-down resistor
	RP22	A22	−	−	−	
	RP23	A23	−	−	−	
	RP24	A24	INTPZ25	−	−	
	RP25	A25	INTPZ26	−	−	
	RP26	A26	INTPZ27	−	−	
	RP27	A27	INTPZ28	−	−	
RP3	RP30	D16/HD16	−	−	−	Hi-Z With internal pull-up resistor
	RP31	D17/HD17	−	−	−	
	RP32	D18/HD18	−	−	−	
	RP33	D19/HD19	−	−	−	
	RP34	D20/HD20	−	−	−	
	RP35	D21/HD21	−	−	−	
	RP36	D22/HD22	−	−	−	
	RP37	D23/HD23	−	−	−	

2.1.5 Serial Flash ROM Interface Signals

The Serial Flash ROM Interface supports Fast Read, Fast Read Dual Output and Fast Read Dual I/O mode.

Pin Name	I/O	Function	Shared Port	Active	Level during reset & Level after reset
SMSCK	O	Serial clock output port for serial flash ROM	P14	↑ / ↓	Hi-Z With internal pull-up resistor
SMSI	I/O	Serial data port for serial flash ROM (Connect to SO of serial flash ROM)	P15	High	
SMSO	I/O	Serial data port for serial flash ROM (Connect to SI of serial flash ROM)	P16	High	
SMCSZ	O	Chip select output port for serial flash ROM	P17	Low	

2.1.6 DMA Interface Signals

There are two DMA Controllers: one with four internal channels but only two external interfaces, and one with one internal channel and one external interce as real-time DMA controller.

Pin Name	I/O	Function	Shared Port	Active	Level during reset & Level after reset
RTDMAREQZ	I	RTDMAC DMA transfer request port	P62	Low	Hi-Z With internal pull-up resistor
RTDMAACKZ	O	RTDMAC DMA acknowledge output port	P63	Low	
RTDMATCZ	O	RTDMAC terminal count output port	P64	Low	
DMAREQZ0	I	DMA transfer request port 0	P65	Low	
DMAACKZ0	O	DMA acknowledge output port 0	P66	Low	
DMATCZ0	O	DMA Terminal count output port 0	P67	Low	
DMAREQZ1	I	DMA transfer request port 1	P32	Low	Hi-Z With internal pull-up resistor
DMAACKZ1	O	DMA acknowledge output port 1	P33	Low	
DMATCZ1	O	DMA Terminal count output port 1	P34	Low	

Caution Each DMA interface is assigned to a specific DMA channel.
DMA channel 0 = interface 0 (DMAREQZ0, DMAACKZ0, DMATCZ0)
DMA channel 1 = interface 1 (DMAREQZ1, DMAACKZ1, DMATCZ1)
DMA channels 2, 3 = no external interface

2.1.7 External Interrupt Input Signals

Pin Name	I/O	Function	Shared Port	Active	Level during reset & Level after reset
NMIZ	I	Non-maskable external interrupt input port	-	Low	Hi-Z High level by internal Pull-up resistor
INTPZ0-INTPZ5	I	External interrupt input port	P00-P05	Low	
INTPZ6, INTPZ7			P12,P13	Low	
INTPZ8-INTPZ10			P22-P24	Low	
INTPZ11			P43	Low	
INTPZ12-INTPZ15			P74-P77	Low	
INTPZ16-INTPZ21			RP00-RP05	Low	
INTPZ22-INTPZ24			P35-P37	Low	
INTPZ25-INTPZ28			RP24-RP27	Low	Hi-Z With internal pull-down resistor

2.1.8 Timer I/O Signals

Pin Name	I/O	Function	Shared Port	Active	Level during reset & Level after reset
TIN0 / TOUT0	I/O	Timer TAUJ0 port	P27	-	Hi-Z With internal pull-up resistor
TIN1 / TOUT1	I/O	Timer TAUJ1 port	P26	-	
TIN2 / TOUT2	I/O	Timer TAUJ2 port	P57	-	Hi-Z With internal pull-up resistor
TIN3 / TOUT3	I/O	Timer TAUJ3 port	P52	-	Hi-Z With internal pull-down resistor

2.1.9 Watchdog Timer Output Signal

Pin Name	I/O	Function	Shared Port	Active	Level during reset & Level after reset
WDTOUTZ	O	Watch Dog Timer output port	P25	Low	Hi-Z With internal pull-up resistor

2.1.10 Trace Signals

Pin Name	I/O	Function	Active	Level during reset & Level after reset
TRACECLK	O	Trace port clock output port	-	-
TRACEDATA3-TRACEDATA0	O	Trace port data output port	-	Low

2.1.11 CPU Power Control Signal

Pin Name	I/O	Function	Shared Port	Active	Level during reset & Level after reset
SLEEPING	O	CPU SLEEP mode output port	P42	High	Hi-Z With internal pull-up resistor

2.1.12 Serial Interface Signals

Pin Name	I/O	Function	Shared Port	Active	Level during reset & Level after reset
TXD0	O	UART0 serial data output port	P21	-	Hi-Z With internal pull-up resistor
RXD0	I	UART0 serial data input port	P20	-	
TXD1	O	UART1 serial data output port	P31	-	
RXD1	I	UART1 serial data input port	P30	-	
CSISCK0	I/O	CSI0 serial clock port	P45	-	
CSISI0	I	CSI0 serial data input port	P46	-	
CSISO0	O	CSI0 serial data output port	P47	-	
CSICS00,CSICS01	O	CSI0 chip select 0,1 port	P70, P71	Low	
CSISCK1	I/O	CSI1 serial clock port	P35	-	
CSISI1	I	CSI1 serial data input port	P36	-	
CSISO1	O	CSI1 serial data output port	P37	-	
CSICS10,CSICS11	O	CSI1 chip select 0,1 port	P72, P73	Low	
SCL0	I/O	I2C0 serial clock port	P60	-	
SDA0	I/O	I2C0 serial data port	P61	-	
SCL1	I/O	I2C1 serial clock port	RP00	-	
SDA1	I/O	I2C1 serial data port	RP01	-	
CRXD0	I	CAN0 receive data port (5V-Tolerant buffer)	P53	-	
CTXD0	O	CAN0 transfer data port	P54	-	
CRXD1	I	CAN1 receive data port (5V-Tolerant buffer)	P55	-	
CTXD1	O	CAN1 transfer data port	P56	-	

2.1.13 CC-Link IE Field Signals (Intelligent device station)

Pin Name	I/O	Function	Shared Port	Active	Level during reset & Level after reset
CCI_RUNLEDZ	O	RUN LED control port	P00	Low	Hi-Z With internal pull-up resistor
CCI_DLINKLEDZ	O	Cyclic communication status check LED control port	P02	Low	
CCI_ERRLEDZ	O	Field Network Error LED control port	P03	Low	
CCI_LERR1LEDZ	O	Link error LED control port 1	P04	Low	
CCI_LERR2LEDZ	O	Link error LED control port 2	P05	Low	
CCI_SDLEDZ	O	Transfer data LED control port	P06	Low	
CCI_RDLEDZ	O	Receive data LED control port	P07	Low	
CCI_NMIZ	O	Output NMI interrupt to MCU	P12	Low	Hi-Z With internal pull-up resistor
CCI_WDTIZ	I	Input from Watchdog Timer	P13	Low	
CCI_WAITEDGEH Note	I/O	Wait Synchronized edge setting 0：rise edge mode 1：low edge mode	P33	-	
CCI_WRLENH Note	I/O	WRL enable setting 0：byte write enable mode 1：byte enable mode	P34	-	
CCI_PHYREZ1	O	PHY reset output 1 port	P56	Low	
CCI_PHYREZ0	O	PHY reset output 0 port	P57	Low	
CCI_INTZ	O	Output Interrupt signal to MCU	P66	Low	
CCI_CLK2_097M	I	2.097152MHz clock	-	-	-

Note. When user does boot with the external memory boot mode, external serial flash ROM boot mode and instruction RAM boot mode, please input high level to P33 and P34 pin during reset.
If you enter a low-level to P33, P34 pin during reset, you can not access the CC-Link IE Field from the CPU of the R-IN32M3.

2.1.14 CC-Link Signals (Intelligent device station)

Pin Name	I/O	Function	Shared Port	Active	Level during reset & Level after reset
CCM_LINKERRZ	O	Link error LED control port	P20	Low	Hi-Z With internal pull-up resistor
CCM_ERRZ	O	Error LED control port	P21	Low	
CCM_RUNZ	O	RUN LED control port	P26	Low	
CCM_MDIN0-CCM_MDIN3	I	Mode setting switch input port	P62-P65	-	
CCM_SNIN0-CCM_SNIN7	I	Station No. setting switch port	P70-P77	-	
CCM_LNKRUNZ	O	Link RUN LED control port	P50	Low	Hi-Z With internal pull-up resistor
CCM_RDLEDZ	O	Receive data LED control port	P51	Low	
CCM_SDLEDZ	O	Transfer data LED control port	RP00	Low	
CCM_IRZ	O	Interrupt output port	P35	Low	
CCM_WDTENZ	I	Watchdog Timer error input port	P13	Low	
CCM_MSTZ	O	Operation check LED port	P37	Low	
CCM_SMSTZ	O	Stand-by master LED control port	RP01	Low	
CCM_RD	I	Data receive port	P53	-	
CCM_SD	O	Data transfer port	P54	-	
CCM_SDGCZ	O	Transfer data & gate control port	P42	Low	
CCM_CLK80M	I	CC-Link Clock	-	-	-

2.1.15 CC-Link Signals (Remote device station)

Caution To use a remote device station, it is necessary to connect a CCS_REFSTB terminal to an external interrupt terminal (INTPZ).

Pin Name	I/O	Function	Shared Port	Active	Level during reset & Level after reset
CCS_MON1- CCS_MON3	O	Monitor port	P32-P34	-	Hi-Z With internal pull-up resistor
CCS_MON4	O	Monitor port	P11	-	Hi-Z With internal pull-down resistor
CCS_MON0	O	Monitor port	P06	-	Hi-Z With internal pull-up resistor
CCS_MON5- CCS_MON7	O	Monitor port	P03-P05	-	
CCS_RESOUT	O	reset port	P07	High	
CCS_IOTENSU	I	Initial setting port	P22	-	
CCS_SENYU0	I	Initial setting port	P23	-	
CCS_SENYU1	I	Initial setting port	P24	-	
CCS_ERRZ	O	Operation check LED port	P25	Low	
CCS_RUNZ	O	Operation check LED port	P26	Low	
CCS_STATION_NO_0- CCS_STATION_NO_7	I	Station No. setting switch port	P70-P77	-	
CCS_LNKRUNZ	O	Link RUN LED control port	P50	Low	Hi-Z With internal pull-up resistor
CCS_REFSTB	O	Interrupt port	P10	High	
CCS_WDTZ	I	Watchdog Timer port	P13	Low	
CCS_RDLEDZ	O	Receive data LED control port	P51	Low	
CCS_RD	I	Data receive port	P53	-	
CCS_SD	O	Data transfer port	P54	-	
CCS_SDLEDZ	O	Operation check LED port	RP00	Low	
CCS_SDGATEON	O	Transfer data & gate control port	P52	High	Hi-Z With internal pull-down resistor
CCS_BS1	I	Baud rate setting switch port	RP02	-	Hi-Z With internal pull-up resistor
CCS_BS2	I	Baud rate setting switch port	RP03	-	
CCS_BS4	I	Baud rate setting switch port	RP04	-	
CCS_BS8	I	Baud rate setting switch port	RP05	-	
CCS_FUSEZ	I	Fuse cutting signal port	P36	Low	
CCM_CLK80M	I	CC-Link clock	-	-	-

2.1.16 System Signals

Pin Name	I/O	Function	Active	Level during reset & Level after reset
XT1	I	Crystal Oscillator ports for system clock	-	-
XT2	I/O	*Oscillator output connects to X2 for direct connection.	-	-
RESETZ	I	Reset input port	Low	-
HOTRESETZ	I	Hot reset Input port	Low	-
PONRZ	I	Internal RAM Power on reset input port	Low	-
OSCTH	I	Input High level when external clock input mode	-	-
JTAGSEL	I	JTAG Operation mode setting port	-	-
RSTOUTZ	O	Reset to external circuit output port	Low	-
CLKOUT25M0	O	PHY clock output port	―	―
CLKOUT25M1	O	PHY clock output port	―	―
PLL_VDD	-	PLL power supply (1.0V)	-	-
PLL_GND	-	PLL power Ground supply (GND)	-	-
VDD33	-	I/O power supply (3.3V)	-	-
VDD10	-	Internal power supply (1.0V)	-	-
GND	-	Ground supply (GND)	-	-
VDDQ_MII	-	Ethernet I/O power supply (3.3V)	-	-

2.1.17 Test Signals

Pin Name	I/O	Function	Active	Level during reset & Level after reset
TMODE0-TMODE2	I	Test mode select port	-	-
TMS	I/O	JTAG mode select port	-	-
TDI	I	JTAG serial data input port	-	-
TDO	O	JTAG serial data output port	-	-
TRSTZ	I	JTAG reset port	Low	-
TCK	I	JTAG clock input port	-	-
TMC1	I	Renesas test ports	-	-
TMC2	I		-	-

2.1.18 Operation mode Setting Signals

Pin Name	I/O	Function	Active	Level during reset & Level after reset
BOOT1-BOOT0	I	Boot mode select port 00 : External memory boot 01 : External serial flash ROM boot 10 : External MCU boot 11 : Instruction RAM boot(debugger used ONLY)	-	-
MEMIFSEL	I	External Memory Interface select port 0 : Slave memory Interface 1 : External MCU Interface	-	-
BUS32EN	I	External Memory Interface Bus width select port 0 : 16bit bus 1 : 32bit bus	-	-
HIFSYNC	I	External MCU I/F Operation mode select port 0 : asynchronous SRAM Interface 1 : synchronous SRAM Interface	-	-
HWRZSEL	I	External MCU Interface HWRZ/HBENZ select port 0 : HBENZ use 1 : HWRZ use	-	-
MEMCSEL	I	Internal Memory Controller select port 0 : asynchronous SRAM MEMC 1 : synchronous burst access MEMC	-	-
ADMUXMODE	I	Multiplex of Address / Data port Note 0 : Separate 1 : Multiplex of Address / Data	-	-

Note. ADMUXMODE port is only available when MEMCSEL port is High (which selects synchronous burst access MEMC). The asynchronous SRAM MEMC does not support address/data multiplexing.

2.2 Port status

The initial status of Port function after the reset cancellation varies according to the status of the operation mode setting signal.

Port Name	External memory boot				External MPU boot		External Serial Flash ROM boot
	Asynchronous MEMC		Synchronous burst MEMC				
	16bit	32bit	16bit	32bit	16bit	32bit	
P14	P14	P14	P14	P14	P14	P14	SMSCK
P15	P15	P15	P15	P15	P15	P15	SMSI
P16	P16	P16	P16	P16	P16	P16	SMSO
P17	P17	P17	P17	P17	P17	P17	SMCSZ
P40	A1	P40	A1	P40	HA1	P40	P40
P41	P41	P41	P41	P41	HWAITZ	HWAITZ	P41
P42	P42	P42	P42	P42	HERROUTZ	HERROUTZ	P42
P43	P43	P43	P43	P43	HBUSCLK	HBUSCLK	P43
P44	P44	P44	P44	P44	HPGCSZ	HPGCSZ	P44
RP06	RP06	WRZ2/ BENZ[note1]	RP06	WRZ2/ BENZ[note1]	RP06	HWRZ2/ HBENZ[note2]	RP06
RP07	RP07	WRZ3/ BENZ[note1]	RP07	WRZ3/ BENZ[note1]	RP07	HWRZ3/ HBENZ[note2]	RP07
RP20	RP20	RP20	ADVZ	ADVZ	HBCYSTZ	HBCYSTZ	RP20
RP10-RP17	RP10-RP17	D24-D31	RP10-RP17	D24-D31	RP10-RP17	HD24-HD31	RP10-RP17
RP30-RP37	RP30-RP37	D16-D23	RP30-RP37	D16-D23	RP30-RP37	HD16-HD23	RP30-RP37

Note1. When using asynchronous SRAM MEMC, WRZ[3:0] and BENZ[3:0] are converted by WREN register. In addition, when using synchronous burst MEMC, WRZ[3:0] and BENZ[3:0] are converted by OPMODE register.

Note2. HWRZ[3:0] and HBENZ[3:0] are converted by the level of HWRZSEL port.

2.3 Operation mode monitor functions

Operation mode setting signals can confirm a setting state by operation mode monitor register.
Operation mode setting signals that can be confirmed are shown below..

Please refer to "R-IN32M3 User's Manual Peripheral functions edition" for the detail of operation mode monitor register.

Table2.1 Operation mode setting signals that can be confirmed

Pin Name	Function
BUS32EN	Select bus width in case of starting external memory I/F
MEMIFSEL	Select a kind of external memory I/F
HIFSYNC	Set operation mode of external MCU I/F
HWRZSEL	Select HWRZ / HBENZ port of external MCU I/F
JTAGSEL	Set operation mode of JTAG port
OSCTH	Input High level in case of external clock input mode¥
BOOT0、BOOT1	Select boot mode
MEMCSEL	Selection of internal memory controller
ADMUXMODE	Set Multiplex of address and data

2.4 Buffer function conversion function

Real-time port signal and apart of port signal can select the drive capability and pulling up / pull-down resistor or not of interface buffer programmably.
This function provides stable operation in system of big load capacity by raising the drive capability.
Please set the buffer function conversion register (DRCTL) to convert the buffer function..

Please refer to "R-IN32M3 User's Manual Peripheral functions edition" for the detail of buffer function conversion register (DRCTL).

2.5 Buffer Types and Recommended Connections for Unused Pins

2.5.1 Ethernet Signals

(1) PHY Interface Signals

Pin Name	I/O	Interface	Recommended connection when not in use
ETH0_TXC	I	Input Buffer (3.3V)	Connect to GND
ETH0_GTXC	O	BID_BUF(3.3V_GMII_MII)_with_IOLH_Control	Open
ETH0_TXEN			
ETH0_TXER			
ETH0_TXD0- ETH0_TXD7			
ETH0_GE_INT	I	Input Buffer (3.3V)	Connect to GND
ETH0_RXC	I	BID_BUF(3.3V_GMII_MII)_with_IOLH_Control	Connect to GND
ETH0_RXDV			
ETH0_RXER			
ETH0_RXD0- ETH0_RXD7			
ETH0_CRS	I	Input Buffer (3.3V)	Connect to GND
ETH0_COL			
ETH1_TXC			
ETH1_GTXC	O	BID_BUF(3.3V_GMII_MII)_with_IOLH_Control	Open
ETH1_TXEN			
ETH1_TXER			
ETH1_TXD0- ETH1_TXD7			
ETH1_GE_INT	I	Input Buffer (3.3V)	Connect to GND
ETH1_RXC	I	BID_BUF(3.3V_GMII_MII)_with_IOLH_Control	Connect to GND
ETH1_RXDV			
ETH1_RXER			
ETH1_RXD0- ETH1_RXD7			
ETH1_CRS	I	Input Buffer (3.3V)	Connect to GND
ETH1_COL			
ETH_MDC	O	Output Buffer (3.3V) 6mA	Open
ETH_MDIO	I/O	I/O Buffer (3.3V) 6mA	Connect to GND

2.5.2 External Memory/ MCU Interface Signals

Pin Name	I/O	Interface	Recommended connection when not in use
BUSCLK	O	Output Buffer (3.3V) 9mA	Open
CSZ0 / HCSZ	I/O	I/O Buffer (3.3V) 6mA 50kΩ Pull-up	Open
A2-A20 / HA2-HA20	I/O	I/O Buffer (3.3V) 6mA 50kΩ Pull-down	Open
D0-D15 / HD0-HD15			
RDZ / HRDZ	I/O	I/O Buffer (3.3V) 6mA 50kΩ Pull-up	Open
WRSTBZ / HWRSTBZ			
WRZ0, WRZ1 / BENZ0, BENZ1 / HWRZ0, HWRZ1			

2.5.3 System Signals

Pin Name	I/O	Interface	Recommended connection when not in use
NMIZ	I	Input Buffer (3.3V) Schmitt in 50kΩ Pull-up	Connect to VDD33(3.3V)
XT1	I	Oscillator with EN	Connect to GND
XT2	-		-
RSTOUTZ	O	Output Buffer (3.3V) 6mA	Open
RESETZ	I	Input Buffer (3.3V) Schmitt in	-
PONRZ			
HOTRESETZ			Connect to VDD33(3.3V)
OSCTH	I	Input Buffer (3.3V) Schmitt in, 50kΩ Pull-down	-
JTAGSEL			
CLKOUT25M0	O	Output Buffer (3.3V) 6mA	Open
CLKOUT25M1			

2.5.4 Test Signals

Pin Name	I/O	Interface	Required Connection when not in use
TMODE0-TMODE2	I	Input Buffer (3.3V) Schmitt in, 50kΩ Pull-down	Connect to GND
TMS	I/O	I/O Buffer (3.3V) 6mA 50kΩ Pull-up	Open
TDI	I	Input Buffer (3.3V) , 50kΩ Pull-up	Open
TDO	O	3-state Output Buffer (3.3V) 6mA	Open
TRSTZ	I	Input Buffer (3.3V) Schmitt in 50kΩ Pull-up	Open
TCK	I	Input Buffer (3.3V) , 50kΩ Pull-down	Open
TMC1	I	(TMC1) Input Buffer (3.3V) for TMC Terminal	Connect to GND
TMC2	I	(TMC2) Input Buffer (3.3V) for TMC Terminal	Connect to GND

2.5.5 Port Signals

(1/2)

Pin Name	I/O	Interface	Recommended connection when not in use
P00-P07 P10	I/O	Programmable I/O Buffer (3.3V) Load Drive select function (6mA, 12mA) Resistor select function (50kΩ Pull-up or 50kΩ Pull-down or less)	Open
P11-P17, P22-P24, P27	I/O	Programmable I/O Buffer (3.3V)(6mA) Resistor select function (50kΩ Pull-up or 50kΩ Pull-down or less)	
P20, P21, P25, P26	I/O	Programmable I/O Buffer (3.3V) Load Drive select function (6mA, 12mA) Resistor select function (50kΩ Pull-up or 50kΩ Pull-down or less)	
P30-P36	I/O	Programmable I/O Buffer (3.3V)(6mA) Resistor select function (50kΩ Pull-up or 50kΩ Pull-down or less)	
P37	I/O	Programmable I/O Buffer (3.3V) Load Drive select function (6mA, 12mA) Resistor select function (50kΩ Pull-up or 50kΩ Pull-down or less)	
P40-P47	I/O	Programmable I/O Buffer (3.3V)(6mA) Resistor select function (50kΩ Pull-up or 50kΩ Pull-down or less)	
P50-P51	I/O	Programmable I/O Buffer (3.3V) Load Drive select function (6mA, 12mA) Resistor select function (50kΩ Pull-up or 50kΩ Pull-down or less)	
P52	I/O	Programmable I/O Buffer (3.3V)(6mA) Resistor select function (50kΩ Pull-up or 50kΩ Pull-down or less)	
P53-P56	I/O	5V-tolerant I/O Buffer 4mA 50kΩ Pull-up	
P57 P60-P67	I/O	Programmable I/O Buffer (3.3V)(6mA) Resistor select function (50kΩ Pull-up or 50kΩ Pull-down or less)	

(2/2)

Pin Name	I/O	Interface	Recommended connection when not in use
P70-P77	I/O	Programmable I/O Buffer (3.3V)(6mA) Resistor select function (50kΩ Pull-up or 50kΩ Pull-down or less)	Open
RP00-RP07 RP10-RP17 RP20-RP27 RP30-RP37	I/O	Programmable I/O Buffer (3.3V) Load Drive select function (6mA, 12mA) Resistor select function (50kΩ Pull-up or 50kΩ Pull-down or less)	

2.5.6 Operation Mode Setting Signals

Pin Name	I/O	Interface	Recommended connection when not in use
BOOT0, BOOT1 MEMIFSEL BUS32EN HIFSYNC HWRZSEL MEMCSEL ADMUXMODE	I	Input Buffer (3.3V) Schmitt in	-

2.5.7 CC-Link IE Field Signal (Intelligent device station)

Pin Name	I/O	Interface	Recommended connection when not in use
CCI_CLK2_097M	I	Input Buffer (3.3V)	2.097152MHz clock input

Caution This pin is needed clock input even if user does not use CC-Link IE Field function.

2.5.8 CC-Link Signal (Intelligent device station, Remote device station)

Pin Name	I/O	Interface	Recommended connection when not in use
CCM_CLK80M	I	Input Buffer (3.3V)	Connect to GND

2.5.9 Trace Signals

Pin Name	I/O	Interface	Recommended connection when not in use
TRACECLK TRACEDATA[3:0]	O	Output Buffer (3.3V) 6mA	Open

3. Memory Maps

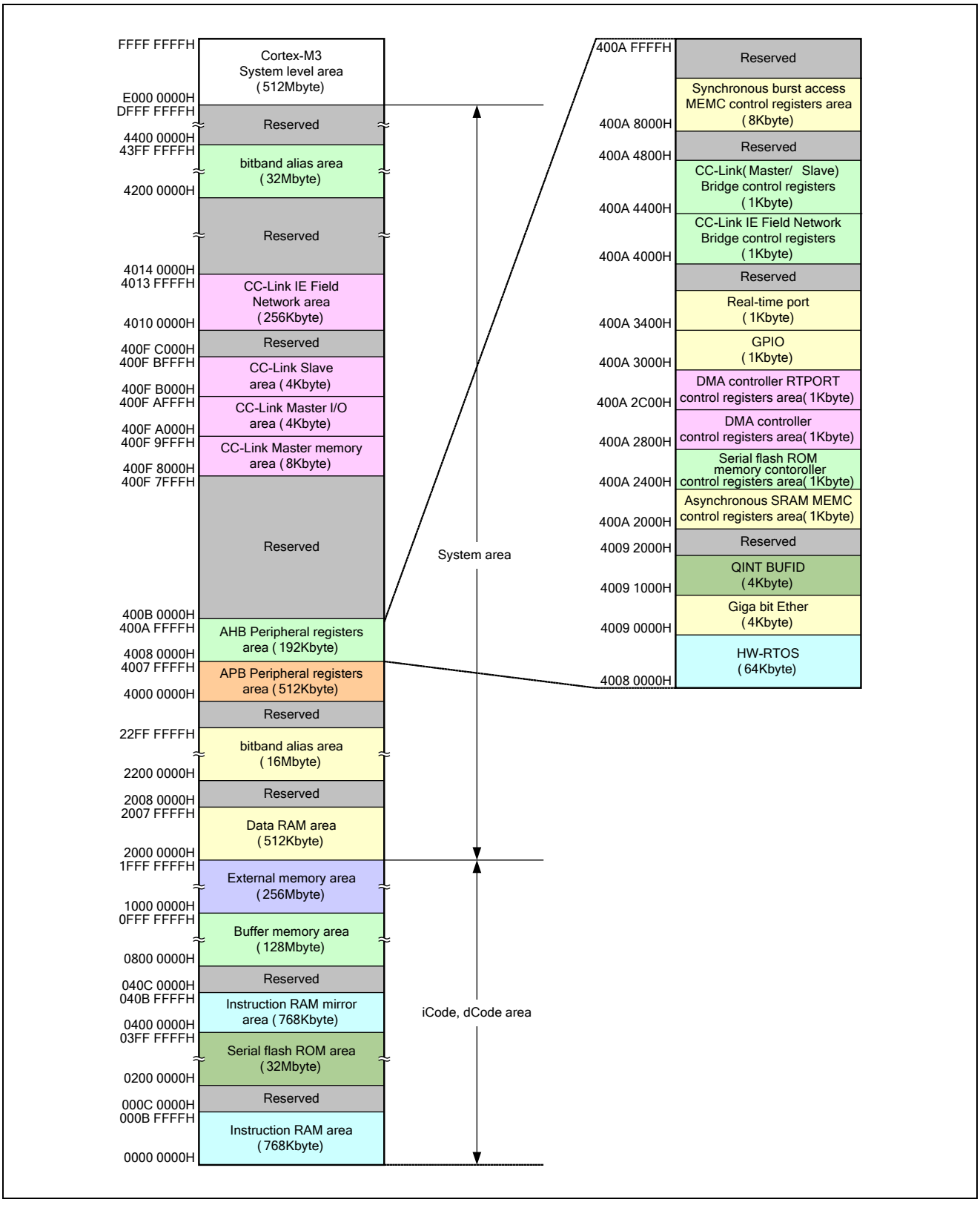


Figure 3.1 Memory map (ALL)

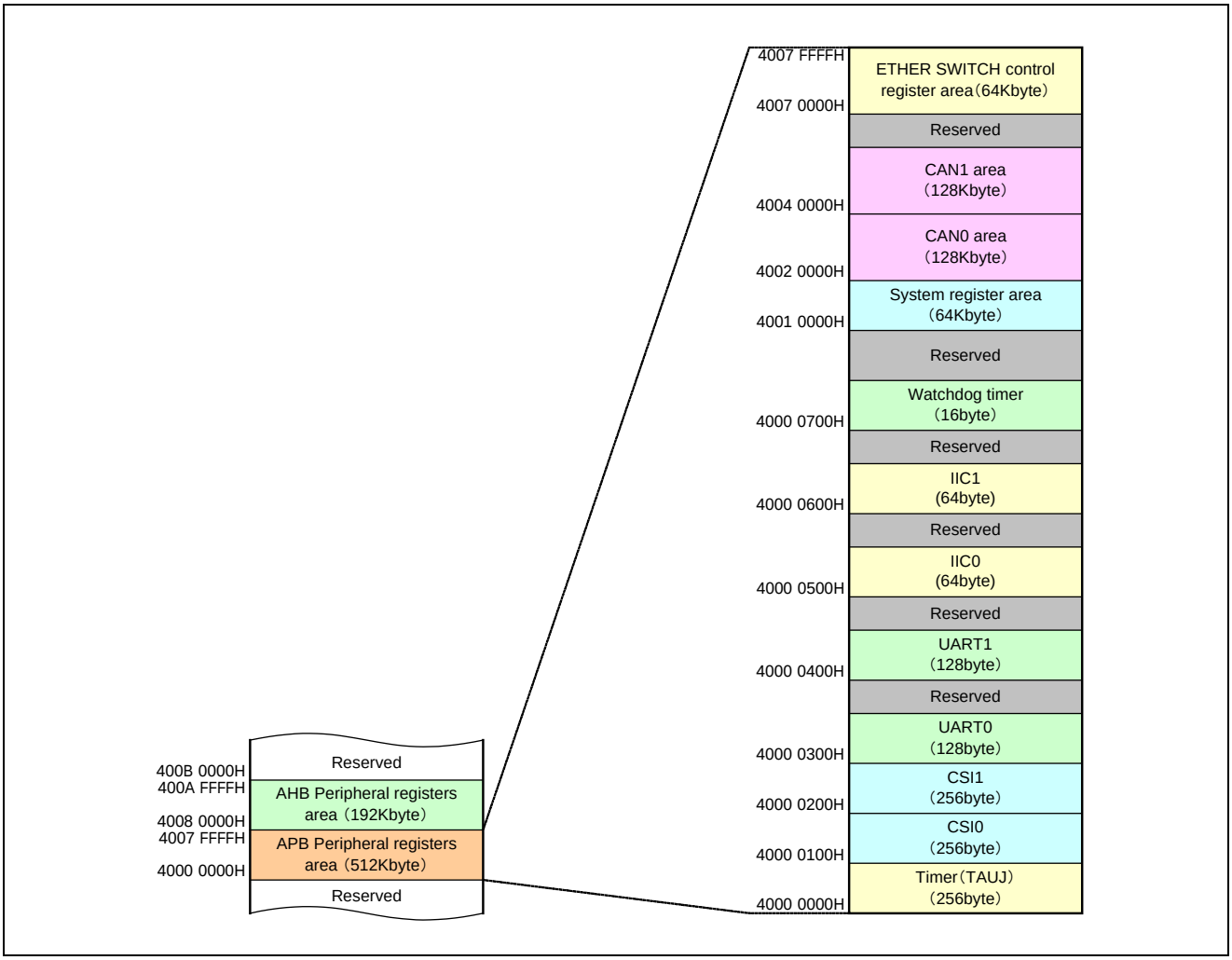


Figure 3.2 Memory map (APB Peripheral registers area)

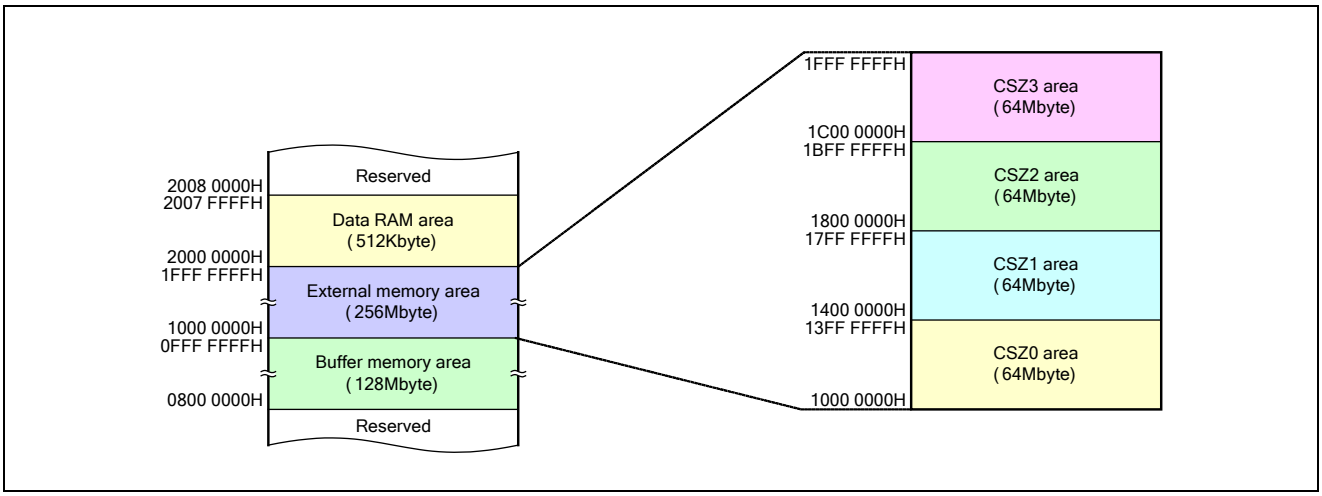


Figure 3.3 Memory map (External memory area)

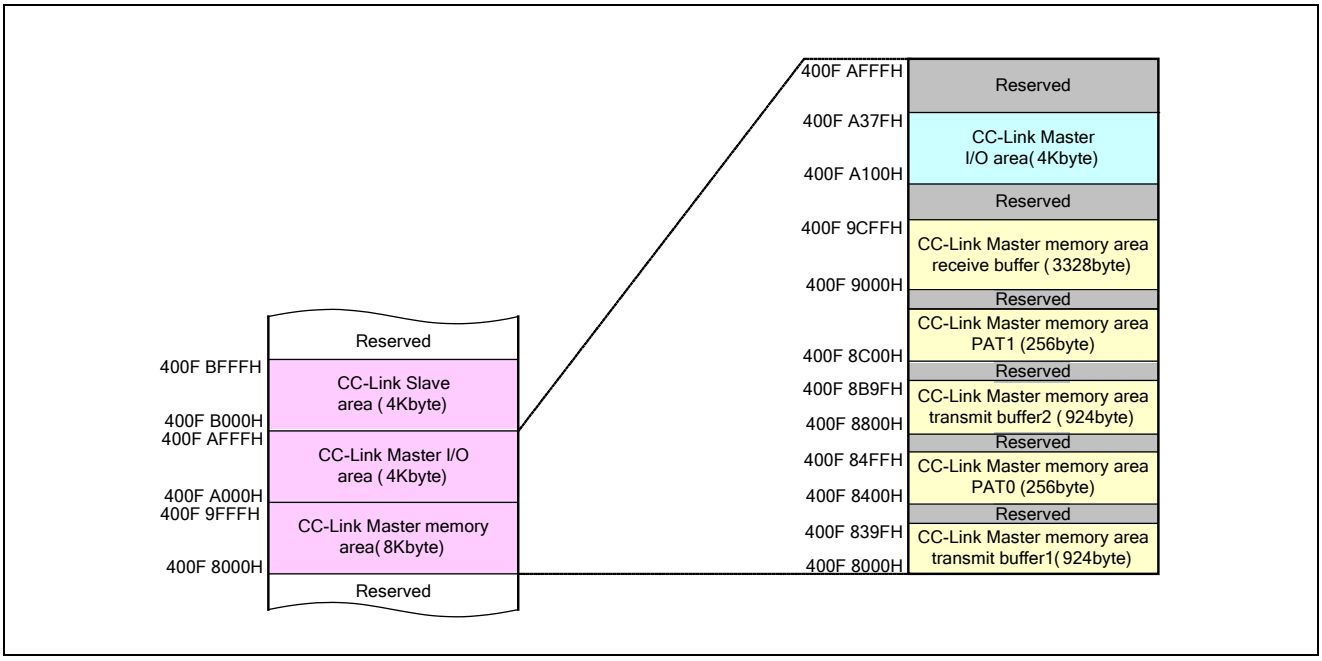


Figure 3.4 Memory map (CC-Link Master area)

Caution1. CC-Link Master shows function block of Intelligent station.

2. CC-Link Slave shows function block of remote device station.

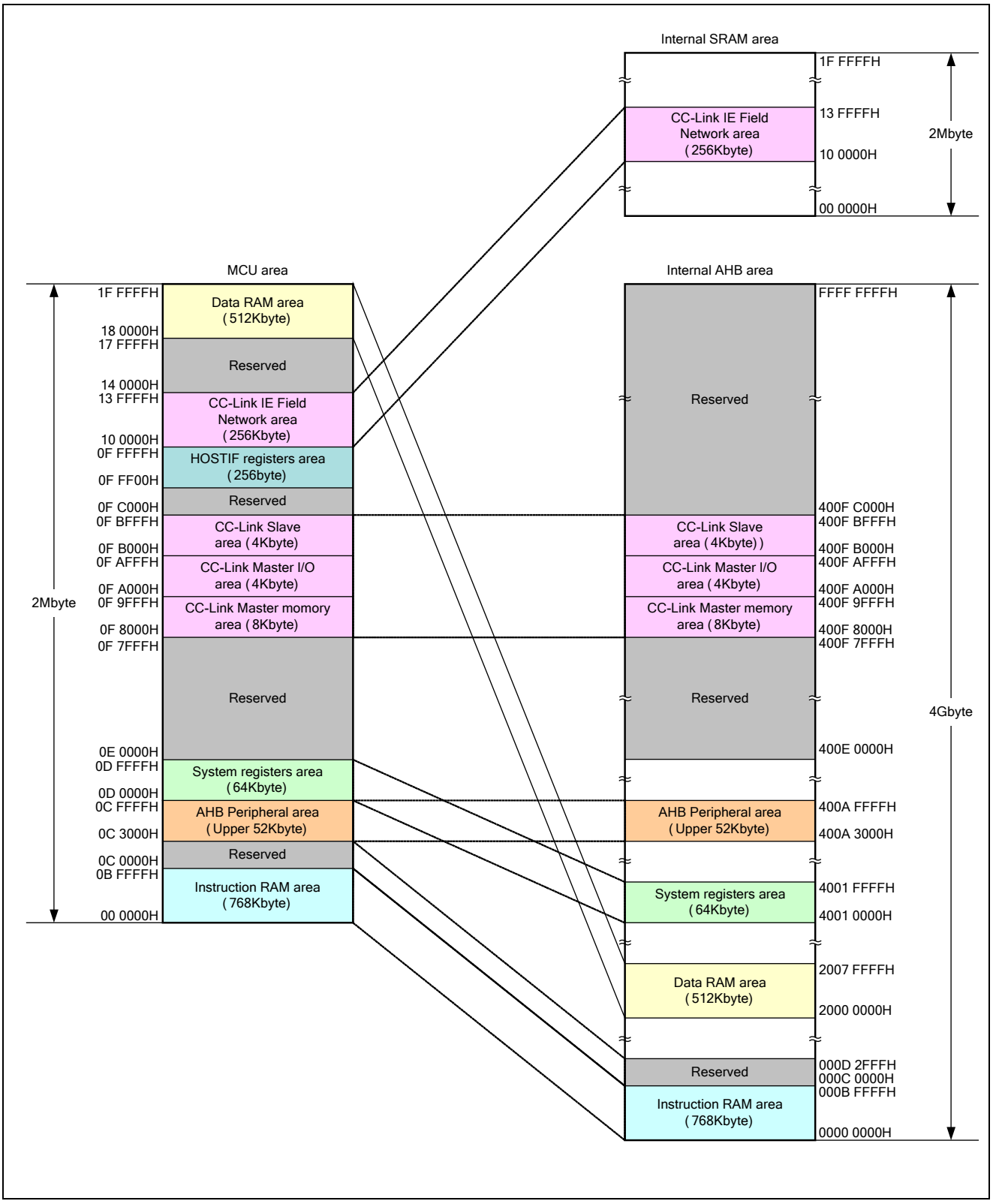


Figure 3.5 External MCU interface area

4. Exception handling function

R-IN32M3 use the Interrupt Controller built-in to Cortex-M3

Please refer to the following URL of ARM for Exceptions handling operation of Cortex-M3.

http://infocenter.arm.com/help/topic/com.arm.doc.set.cortexm/index.html

4.1 Exceptions list

Exception No.1-15 is system exception of Cortex-M3 CPU. The interrupt from the internal hardware of R-IN32M3 and External port is assigned after Exception No.16.

Exception No.	Exception type	Priority	Remark
1	Reset	-3 (most significant)	-Reset port (RST_B) input -Reset from Watchdog Timer -Set (1) the SYSRESETREQ bit of NVIC built-in Cortex-M3 CPU
2	NMI	-2	-NMI port input -Generate NMI from Watchdog Timer
3	Hard fault	-1	Using to the promotion of exception fault of all class that can be operated by other exceptions.
4	Memory manage fault	programmable	Exception from MPU
5	Bus fault	programmable	Bus error of bus access to the area that is not controlled by MPU
6	Use fault	programmable	Error about operating instruction including undefined instruction
7~10	Reserved	-	-
11	SVCall	programmable	Call of system service by SVC interrupt
12	Debug Monitor	programmable	Debug Monitor
13	Reserved	-	-
14	PendSV	programmable	Request to system service that can be reserved
15	SysTick	programmable	Indication from system timer
16~	R-IN32M3 specific Interrupt	programmable	Interrupt from the internal hardware of R-IN32M3 and external port.

4.2 Interrupt list

These interrupts are exceptions(interrupt) after the Exception No.16 that are assigned NVIC of Cortex-M3 CPU.

In R-IN32M3, the interrupts from the internal hardware of R-IN32M3 and external port connect to not only NVIC of Cortex-M3 but also the internal Hardware Real-time OS, starting trigger of internal DMAC and timer.

R-IN32M3 supports the following interrupts.

Table4.1 Interrupt list

(1/4)

Exception No.	Name	Cause group	Connection				
			NVIC	HW-RTOS	DMAC	Real Time Port	Timer
16	INTTAUJ2I0	Timer array TAUJ2 channel 0 interrupt	○	○	○	○	○
17	INTTAUJ2I1	Timer array TAUJ2 channel 1 interrupt	○	○	○	○	○
18	INTTAUJ2I2	Timer array TAUJ2 channel 2 interrupt	○	○	○	○	○
19	INTTAUJ2I3	Timer array TAUJ2 channel 3 interrupt	○	○	○	○	○
20	INTUAJ0TIT	UARTJ0 transmission interrupt	○	○	○	○	○
21	INTUAJ0TIR	UARTJ0 reception interrupt	○	○	○	○	○
22	INTUAJ1TIT	UARTJ1 transmission interrupt	○	○	○	○	○
23	INTUAJ1TIR	UARTJ1 reception interrupt	○	○	○	○	○
24	INTCSIH0IC	CSIH0 communication status interrupt	○	○	○	○	○
25	INTCSIH0IR	CSIH0 reception status interrupt	○	○	○	○	○
26	INTCSIH0IJC	CSIH0 end of job interrupt	○	○	○	○	○
27	INTCSIH1IC	CSIH1 communication status interrupt	○	○	○	○	○
28	INTCSIH1IR	CSIH1 reception status interrupt	○	○	○	○	○
29	INTCSIH1IJC	CSIH1 end of job interrupt	○	○	○	○	○
30	INTIICB0TIA	IICB0 transmission/reception interrupt request	○	○	○	○	○
31	INTIICB1TIA	IICB1 transmission/reception interrupt request	○	○	○	○	○
32	INTFCN0REC	FCN0 reception completion	○	○	○	○	○
33	INTFCN0TRX	FCN0 transmission completion	○	○	○	○	○
34	INTFCN0WUP	FCN0 sleep and wakeup / transmission suspension	○	○	○	○	○
35	INTFCN1REC	FCN1 reception completion	○	○	○	○	○
36	INTFCN1TRX	FCN1 transmission completion	○	○	○	○	○
37	INTFCN1WUP	FCN1 sleep and wakeup / transmission suspension	○	○	○	○	○
38	INTDMA00	DMAC channel0 transfer completion interrupt	○	○	○	○	○
39	INTDMA01	DMAC channel1 transfer completion interrupt	○	○	○	○	○
40	INTDMA02	DMAC channel2 transfer completion interrupt	○	○	○	○	○
41	INTDMA03	DMAC channel3 transfer completion interrupt	○	○	○	○	○
42	INTRTDMA	RTDMAC transfer completion interrupt	○	○	○	○	○
43	-	Reserve	-	-	-	-	-
44	-	Reserve	-	-	-	-	-
45	-	Reserve	-	-	-	-	-

(2/4)

Exception No.	Name	Cause group	Connection				
			NVIC	HW-RTOS	DMAC	Real Time Port	Timer
46	-	Reserve	-	-	-	-	-
47	-	Reserve	-	-	-	-	-
48	INTBUFDMA	Inter-Buffer DMA transfer completion	○	○	○	○	○
49	INTPHY0	Ether PHYinterrupt0	○	○	○	○	○
50	INTPHY1	Ether PHYinterrupt1	○	○	○	○	○
51	INTETHMII	Ether MII management access completion interrupt	○	○	○	○	○
52	INTETHPAUSE	Ether pause packet transmission completion	○	○	○	○	○
53	INTETHTX	Ether transmission completion interrupt	○	○	○	○	○
54	INTETHSW	Ether SWITCH interrupt	○	○	○	○	○
55	INTETHSWDLR	Ether SWITCH DLR interrupt	○	○	○	○	○
56	INTETHSWSEC	Ether SWITCH SEC interrupt	○	○	○	○	○
57	INTETHRXFIFO	RX FIFO overflow	○	○	-	-	-
58	INTETHTXFIFO	TX FIFO underflow	○	○	-	-	-
59	INTETHRXDMA	Ether MACDMA reception completion	○	○	○	○	○
60	INTETHTXDMA	Ether MACDMA transmission completion	○	○	○	○	○
61	INTMACDMARXFRM	receive frame successfully interrupt	○	○	○	○	○
62	INTHOSTIF	External MCU I/F interrupt	○	○	○	○	○
63	INTPZ0	INTPZ0 input	○	○	○	○	○
64	INTPZ1	INTPZ1 input	○	○	○	○	○
65	INTPZ2	INTPZ2 input	○	○	○	○	○
66	INTPZ3	INTPZ3 input	○	○	○	○	○
67	INTPZ4	INTPZ4 input	○	○	○	○	○
68	INTPZ5	INTPZ5 input	○	○	○	○	○
69	INTPZ6	INTPZ6 input	○	○	○	○	○
70	INTPZ7	INTPZ7 input	○	○	○	○	○
71	INTPZ8	INTPZ8 input	○	○	○	○	○
72	INTPZ9	INTPZ9 input	○	○	○	○	○
73	INTPZ10	INTPZ10 input	○	○	○	○	○
74	INTPZ11	INTPZ11 input	○	○	○	○	○
75	INTPZ12	INTPZ12 input	○	○	○	○	○
76	INTPZ13	INTPZ13 input	○	○	○	○	○
77	INTPZ14	INTPZ14 input	○	○	○	○	○
78	INTPZ15	INTPZ15 input	○	○	○	○	○
79	INTPZ16	INTPZ16 input	○	○	○	○	○
80	INTPZ17	INTPZ17 input	○	○	○	○	○
81	INTPZ18	INTPZ18 input	○	○	○	○	○
82	INTPZ19	INTPZ19 input	○	○	○	○	○

(3/4)

Exception No.	Name	Cause group	Connection				
			NVIC	HW-RTOS	DMAC	Real Time Port	Timer
83	INTPZ20	INTPZ20 input	○	○	○	○	○
84	INTPZ21	INTPZ21 input	○	○	○	○	○
85	INTPZ22	INTPZ22 input	○	○	○	○	○
86	INTPZ23	INTPZ23 input	○	○	○	○	○
87	INTPZ24	INTPZ24 input	○	○	○	○	○
88	INTPZ25	INTPZ25 input	○	○	○	○	○
89	INTPZ26	INTPZ26 input	○	○	○	○	○
90	INTPZ27	INTPZ27 input	○	○	○	○	○
91	INTPZ28	INTPZ28 input	○	○	○	○	○
92	INTHWRTOS	HW-RTOS interrupt	○	-	-	-	-
93	INTBRAMERR	Buffer RAM area access error	○	○	-	-	-
94	INTIICB0TIS	I2C0 status interrupt	○	○	-	-	-
95	INTIICB1TIS	I2C1 status interrupt	○	○	-	-	-
96	-	Reserve	-	-	-	-	-
97	INTSFLASH	Serial Flash ROM controller error interrupt	○	○	-	-	-
98	INTUAJ0TIS	UARTJ0 status interrupt	○	○	-	-	-
99	INTUAJ1TIS	UARTJ1 status interrupt	○	○	-	-	-
100	INTCSIH0IRE	CSIH0 communication error interrupt	○	○	-	-	-
101	INTCSIH1IRE	CSIH1 communication error interrupt	○	○	-	-	-
102	INTFCN0ERR	FCN0 error detection	○	○	-	-	-
103	INTFCN1ERR	FCN1 error detection	○	○	-	-	-
104	INTDERR0	DMAC error response interrupt	○	○	-	-	-
105	INTDERR1	RTDMAC error response interrupt	○	○	-	-	-
106	INTETHTXFIFOERR	TX-FIFO error interrupt	○	○	-	-	-
107	INTETHRXERR	Ether receive flame error	○	○	-	-	-
108	INTETHRXDERR	MACDMA reception error interrupt	○	○	-	-	-
109	INTETHTXDERR	MACDMA transmission error interrupt	○	○	-	-	-
110	INTBUFDMAERR	Internal Buffer DMA error	○	○	-	-	-
111	-	Reserve	-	-	-	-	-
112	-	Reserve	-	-	-	-	-
113	-	Reserve	-	-	-	-	-
114	-	Reserve	-	-	-	-	-
115	-	Reserve	-	-	-	-	-
116	-	Reserve	-	-	-	-	-
117	-	Reserve	-	-	-	-	-
118	-	Reserve	-	-	-	-	-
119	-	Reserve	-	-	-	-	-

(4/4)

Exception No.	Name	Cause group	Connection				
			NVIC	HW-RTOS	DMAC	Real Time Port	Timer
120	-	Reserve	-	-	-	-	-
121	INTCCISYCO	CC-Link IE Synco interrupt	○	○	○	○	○
122	INTCCISYNCI	CC-Link IE Synci interrupt	○	○	○	○	○
123	INTCCINMIZ	CC-Link IE NMIZ interrupt	○	○	○	○	○
124	INTCCIWDTZ	CC-Link IE WDTZ interrupt	○	○	○	○	○
125	INTCCIINTZ	CC-Link IE INTZ interrupt	○	○	○	○	○
126	INTCCICLKLOSSZ	CC-Link IE CLKLOSSZ interrupt	○	○	○	○	○
127	INTCCIMON0	CC-Link IE MON0 interrupt	○	○	○	○	○
128	INTCCIMON1	CC-Link IE MON1 interrupt	○	○	○	○	○
129	INTCCIMON2	CC-Link IE MON2 interrupt	○	○	○	○	○
130	INTCCIMON3	CC-Link IE MON3 interrupt	○	○	○	○	○
131	INTCCMRQ	CC-Link INTRQ interrupt	○	○	○	○	○
132	INTCCSRFSTB	CC-Link RFSTB interrupt	○	○	○	○	○
133	INTCCSMON3	CC-Link MON3 interrupt	○	○	○	○	○

Note To use a CC-Link remote device station(V2.0), INTCCSRFSTB can not be used. It is necessary to connect a CCS_REFSTB(P10) terminal to an external interrupt terminal (INTPZ).

5. Peripheral function

Please refer to "R-IN32M3 User's Manual Peripheral functions edition" for the detail of following peripheral functions.

- Clock function
- CPU
- Bus structure
- Hardware Real-time OS
- Giga bit Ethernet I/F
- Asynchronous SRAM MEMC
- Synchronous burst access MEMC
- Serial Flash ROM MEMC
- DMA function
- Timer Array Unit J (TAUJ)
- Window Watchdog Timer A (WDTA)
- Asynchronous Serial Interface J (UARTJ)
- Clocked Serial Interface H (CSIH)
- I^2C BUS (IICB)
- CAN Controller (FCN)
- CC-Link (Intelligent device station)
- CC-Link (Remote device station)
- Other I/F control
- Debug function

6. CC-Link IE Field (Intelligent device station) Function

The outline specifications of CC-Link IE Field are as follows.
Please refer to the following URL of CLPA for additional details and specifications for the CC-Link IE Field core.

http://www.cc-link.org/jp/cclink/cclinkie/index.html

Table 6.1 CC-Link IE Field outline specifications

Item	Specification
Ethernet Standards	IEEE802.3ab (1000BASE-T) compliant
Communication speed	1Gbps
Topology	Line, star, ring
Maximum number of connected units	254 modules (total of master and slave stations)
Maximum station-to-station distance	100m

6.1 CC-Link IE Field (Intelligent device station) control register

This register is the control register to adjust the access timing from CPU to CC-Link IE Field core.

Table 6.2 CC-Link IE Field (Intelligent device station) control registers overview

Register name	Shortcut	Address
CC-Link IE Field (Intelligent device station) clock gata register	CIECLKGTD	4001 0938H
CC-Link IE Field (Intelligent device station) wait delay register	CIEWAITDLY	4001 093CH
CC-Link IE Field (Intelligent device station) bus size control register	CIEBSC	400A 4004H
CC-Link IE Field (Intelligent device station) bus bridge control register	CIESMC	400A 4008H

6.1.1 CC-Link IE Field (Intelligent device station) clock gate register（CIECLKGTD）

CIECLKGTD register is used to temporarily stop the supply of the bus clock to prevent a clock glitch that occurs to the bus clock switching when the CC-Link IE Field Network. Stop the bus clock by writing 1 to this register, and then restart the bus clock by writing 0. The case of switching to enable the SRAM bus path from the external microcomputer, to switch shown to first stop bus clock in this register always.

- Access This register can be read and written in 32-bit or 16-bit units.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
CIECLKGTD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CIECLKGTD	4001 0938H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	Initial Value 0000 0000H

Bit position	Bit name	Function
0	CIECLKGTD	Stop the bus clock of the CC-Link IE Field Network. 0：Provide operation bus clock 1：Stop operation bus clock

6.1.2 CC-Link IE Field (Intelligent device station) wait delay register（CIEWAITDLY）

CIEWAITDLY register is used to extend the wait period cycle to the bus of the CC-Link IE Field Network. Can be set up to 4 cycles from 0 cycle. The setting of this register should be set before the start accessing the CC-Link IE Field Network.

- Access This register can be read and written in 32-bit or 16-bit units.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
CIEWAITDLY	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	WAITDLY2	WAITDLY1	WAITDLY0	4001 093CH
																																	Initial Value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	0000 0000H

Bit position	Bit name	Function
2-0	WAITDLY2-0	Sets a the wait period cycle to the bus of the CC-Link IE Field Network. 000 : 4 X HBUSCLK (initial value) 001 : 3 X HBUSCLK 010 : 2 X HBUSCLK 011 : 1 X HBUSCLK 100 : 0 X HBUSCLK (through) Other : It is the forbidden BUSCLK.

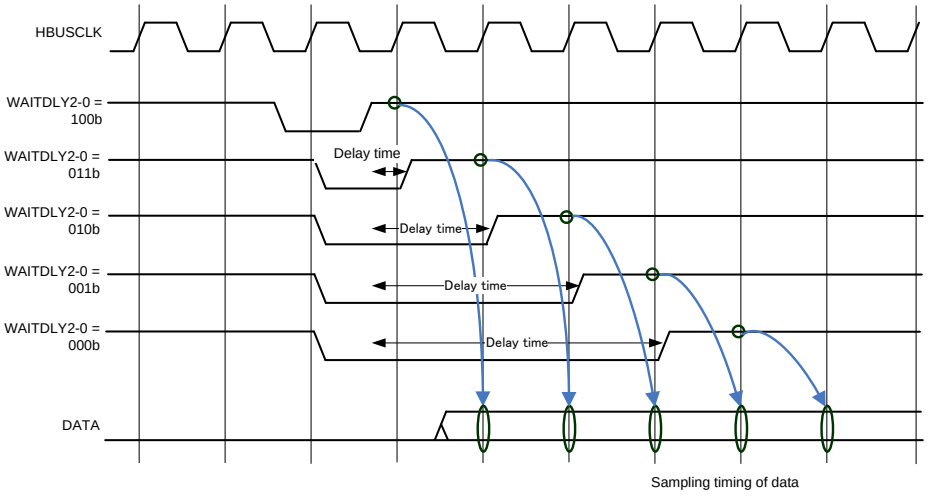


Figure 6.1 Data sampling timing example

6.1.3 CC-Link IE Field (Intelligent device station) bus size control register (CIEBSC)

CIEBSC register set the data bus width to access CC-Link IE Field (Intelligent device station) core. This register must be fixed to 0000 5555H in case of using CC-Link IE Field (Intelligent device station).

- Access This register can be read/written in 32-bit units.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
CCBSC	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	400A 4004H
																																	Initial Value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0000 5555H

Bit position	Bit name	Function
31-0	-	This register must be fixed to 0000 5555H.

6.1.4 CC-Link IE Field (Intelligent device station) bus bridge control register (CIESMC)

CIESMC register controls to access. This register must be fixed to 0000 1151H in case of using CC-Link IE Field (Intelligent device station)..

- Access This register can be read/written in 32-bit units.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
CIESMC	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	0	1	0	0	0	1	400A 4008H
																																	Initial Value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	0	1	0	0	0	1	0000 FFFFH

Bit position	Bit name	Function
31-0	-	This register must be fixed to 0000 1151H

7. Port function

7.1 Features

- Number of I/O ports: 96
- Can function alternately as the I/O pins of other peripheral functions.
- Input or output can be specified by bit unit.

Caution 1. If a signal from a peripheral function pin that functions alternately as a port pin is switched to port mode by changing the PMCn register setting, a spike might occur, depending on the pin status at that time.
The following general countermeasure for spikes should therefore be implemented by software.

- **Switch the pin function while the peripheral function is stopped.**
- **For pins that function alternately as interrupt signal pins, clear the interrupt request flag, and then cancel masking of the interrupt.**
- **Wait until the output value stabilizes and then switch the mode.**

2. Do not externally input an intermediate voltage to input buffers because these buffers do not implement through-current countermeasures.

7.2 Port configuration

The R-IN32M3-CL incorporates eight ports of 3-state I/O port and four real-time control ports. Input or output mode can be specified for ports in 1-bit units. Each port basically consists of 8 bits, but ports 0 to 3 can also be aligned to enable reading and writing in 32-bit units. The real-time ports (RP00 to RP37) can be used for I/O in synchronization with interrupt signals.

Each port has the registers shown below, each of which is used to set the I/O mode and specify the use of the alternate function of the port. The basic circuit configuration is shown in Figure 7.1.

Register name	Purpose and operation	
	Read	Write
Port registers (Pn, RPm)	Used to read the value of the output latch.	Used to set a value to the output latch.
Port mode registers (PMn, RPMm)	Used to read whether the port is in input or output mode.	Used to set the port to input or output mode.
Port mode control registers (PMCn, RPMCm)	Used to read whether the port is used as a port or as an alternate function pin.	Used to specify whether to use a port as a port or for an alternate function.
Port function control registers (PFCn, RPFCm)	Used to read which alternate function of the port is selected, if the port has more than one alternate function.	Used to specify which alternate function of the port to be selected, if the port has more than one alternate function.
Port function control expansion registers (PFCEn, RPFCEm)	Used to read which alternate function of the port is selected, if the port has more than two alternate functions.	Used to specify which alternate function of the port to be selected in combination with the PFCn register setting, if the port has more than two alternate functions.
Port pin input registers (PINn, RPINm)	Used to read the input level of the port pin.	Cannot be written.

Caution If a port that has multiple alternate functions, including external interrupt input, is set to control mode by using the PMCn register, and if the alternate function is used in input mode, the external interrupt input is also shared.

Remark n = 0 to 7, m = 0 -3

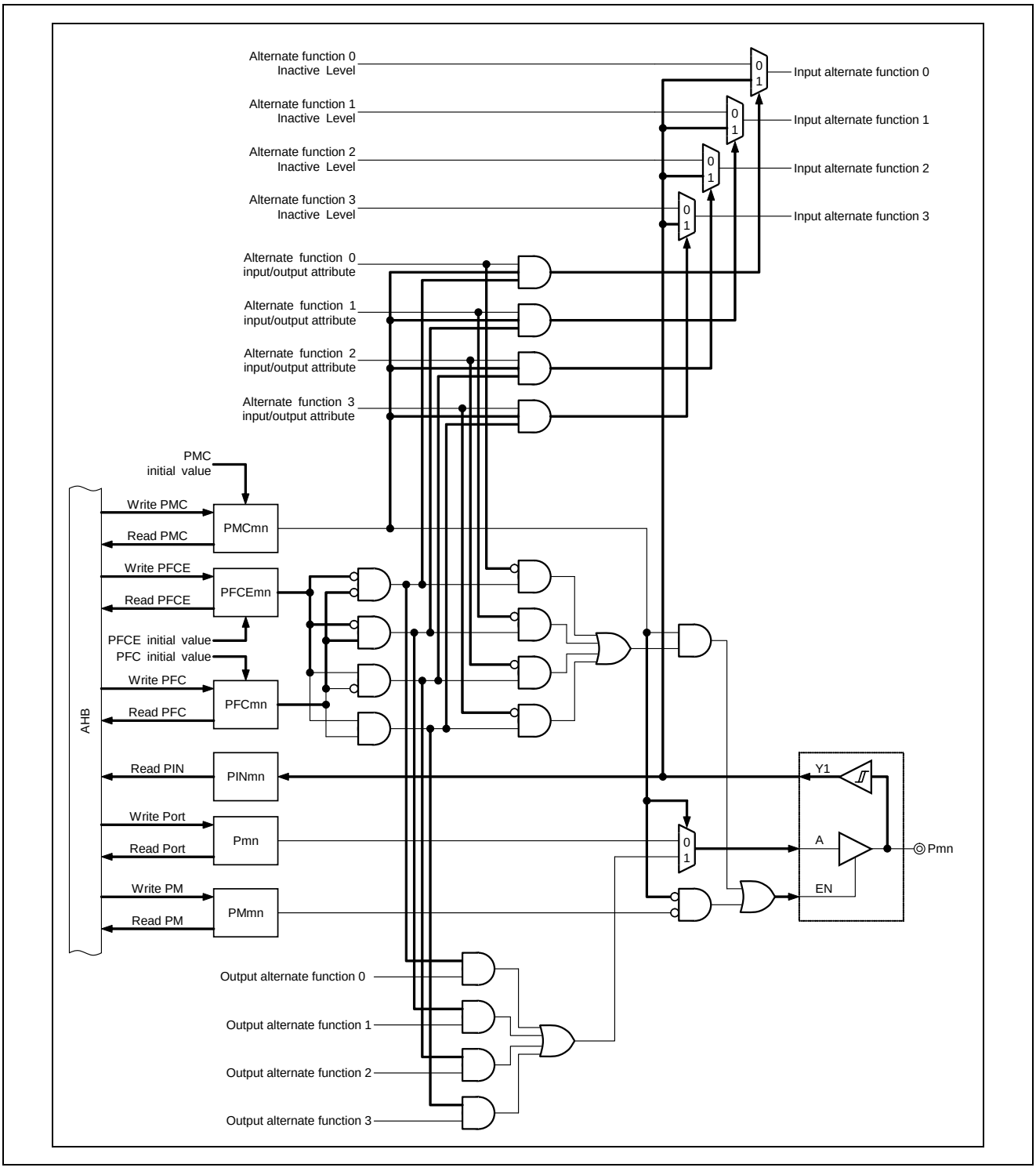


Figure 7.1 Basic port circuit configuration

7.3 Registers

(1/6)

Register name	Symbol	Address
Port register 0 (8 bits)	P0B	400A 3000H
Port register 1 (8 bits)	P1B	400A 3001H
Port register 2 (8 bits)	P2B	400A 3002H
Port register 3 (8 bits)	P3B	400A 3003H
Port register 4 (8 bits)	P4B	400A 3004H
Port register 5 (8 bits)	P5B	400A 3005H
Port register 6 (8 bits)	P6B	400A 3006H
Port register 7 (8 bits)	P7B	400A 3007H
Port register 0 (16 bits)	P0H	400A 3000H
Port register 2 (16 bits)	P2H	400A 3002H
Port register 4 (16 bits)	P4H	400A 3004H
Port register 6 (16 bits)	P8H	400A 3006H
Port register 0 (32 bits)	P0W	400A 3000H
Port register 4 (32 bits)	P4W	400A 3004H
Port mode register 0 (8 bits)	PM0B	400A 3010H
Port mode register 1 (8 bits)	PM1B	400A 3011H
Port mode register 2 (8 bits)	PM2B	400A 3012H
Port mode register 3 (8 bits)	PM3B	400A 3013H
Port mode register 4 (8 bits)	PM4B	400A 3014H
Port mode register 5 (8 bits)	PM5B	400A 3015H
Port mode register 6 (8 bits)	PM6B	400A 3016H
Port mode register 7 (8 bits)	PM7B	400A 3017H
Port mode register 0 (16 bits)	PM0H	400A 3010H
Port mode register 2 (16 bits)	PM2H	400A 3012H
Port mode register 4 (16 bits)	PM4H	400A 3014H
Port mode register 6 (16 bits)	PM6H	400A 3016H
Port mode register 0 (32 bits)	PM0W	400A 3010H
Port mode register 4 (32 bits)	PM4W	400A 3014H

(2/6)

Register name	Symbol	Address
Port mode control register 0 (8 bits)	PMC0B	400A 3020H
Port mode control register 1 (8 bits)	PMC1B	400A 3021H
Port mode control register 2 (8 bits)	PMC2B	400A 3022H
Port mode control register 3 (8 bits)	PMC3B	400A 3023H
Port mode control register 4 (8 bits)	PMC4B	400A 3024H
Port mode control register 5 (8 bits)	PMC5B	400A 3025H
Port mode control register 6 (8 bits)	PMC6B	400A 3026H
Port mode control register 7 (8 bits)	PMC7B	400A 3027H
Port mode control register 0 (16 bits)	PMC0H	400A 3020H
Port mode control register 2 (16 bits)	PMC2H	400A 3022H
Port mode control register 4 (16 bits)	PMC4H	400A 3024H
Port mode control register 6 (16 bits)	PMC6H	400A 3026H
Port mode control register 0 (32 bits)	PMC0W	400A 3020H
Port mode control register 4 (32 bits)	PMC4W	400A 3024H
Port function control register 0 (8 bits)	PFC0B	400A 3030H
Port function control register 1 (8 bits)	PFC1B	400A 3031H
Port function control register 2 (8 bits)	PFC2B	400A 3032H
Port function control register 3 (8 bits)	PFC3B	400A 3033H
Port function control register 4 (8 bits)	PFC4B	400A 3034H
Port function control register 5 (8 bits)	PFC5B	400A 3035H
Port function control register 6 (8 bits)	PFC6B	400A 3036H
Port function control register 7 (8 bits)	PFC7B	400A 3037H
Port function control register 0 (16 bits)	PFC0H	400A 3030H
Port function control register 2 (16 bits)	PFC2H	400A 3032H
Port function control register 4 (16 bits)	PFC4H	400A 3034H
Port function control register 6 (16 bits)	PFC6H	400A 3036H
Port function control register 0 (32 bits)	PFC0W	400A 3030H
Port function control register 4 (32 bits)	PFC4W	400A 3034H

(3/6)

Register name	Symbol	Address
Port function control expansion register 0 (8 bits)	PFCE0B	400A 3040H
Port function control expansion register 1 (8 bits)	PFCE1B	400A 3041H
Port function control expansion register 2 (8 bits)	PFCE2B	400A 3042H
Port function control expansion register 3 (8 bits)	PFCE3B	400A 3043H
Port function control expansion register 4 (8 bits)	PFCE4B	400A 3044H
Port function control expansion register 5 (8 bits)	PFCE5B	400A 3045H
Port function control expansion register 6 (8 bits)	PFCE6B	400A 3046H
Port function control expansion register 7 (8 bits)	PFCE7B	400A 3047H
Port function control expansion register 0 (16 bits)	PFCE0H	400A 3040H
Port function control expansion register 2 (16 bits)	PFCE2H	400A 3042H
Port function control expansion register 4 (16 bits)	PFCE4H	400A 3044H
Port function control expansion register 6 (16 bits)	PFCE6H	400A 3046H
Port function control expansion register 0 (32 bits)	PFCE0W	400A 3040H
Port function control expansion register 4 (32 bits)	PFCE4W	400A 3044H
Port pin input register 0 (8 bits)	PIN0B	400A 3050H
Port pin input register 1 (8 bits)	PIN1B	400A 3051H
Port pin input register 2 (8 bits)	PIN2B	400A 3052H
Port pin input register 3 (8 bits)	PIN3B	400A 3053H
Port pin input register 4 (8 bits)	PIN4B	400A 3054H
Port pin input register 5 (8 bits)	PIN5B	400A 3055H
Port pin input register 6 (8 bits)	PIN6B	400A 3056H
Port pin input register 7 (8 bits)	PIN7B	400A 3057H
Port pin input register 0 (16 bits)	PIN0H	400A 3050H
Port pin input register 2 (16 bits)	PIN2H	400A 3052H
Port pin input register 4 (16 bits)	PIN4H	400A 3054H
Port pin input register 6 (16 bits)	PIN6H	400A 3056H
Port pin input register 0 (32 bits)	PIN0W	400A 3050H
Port pin input register 4 (32 bits)	PIN4W	400A 3054H

(4/6)

Register name	Symbol	Address
RT port register 0 (8 bits)	RP0B	400A 3400H
RT port register 1 (8 bits)	RP1B	400A 3401H
RT port register 2 (8 bits)	RP2B	400A 3402H
RT port register 3 (8 bits)	RP3B	400A 3403H
RT port register 0 (16 bits)	RP0H	400A 3400H
RT port register 2 (16 bits)	RP2H	400A 3402H
RT port register 0 (32 bits)	RP0W	400A 3400H
RT port mode register 0 (8 bits)	RPM0B	400A 3410H
RT port mode register 1 (8 bits)	RPM1B	400A 3411H
RT port mode register 2 (8 bits)	RPM2B	400A 3412H
RT port mode register 3 (8 bits)	RPM3B	400A 3413H
RT port mode register 0 (16 bits)	RPM0H	400A 3410H
RT port mode register 2 (16 bits)	RPM2H	400A 3412H
RT port mode register 0 (32 bits)	RPM0W	400A 3410H
RT port mode control register 0 (8 bits)	RPMC0B	400A 3420H
RT port mode control register 1 (8 bits)	RPMC1B	400A 3421H
RT port mode control register 2 (8 bits)	RPMC2B	400A 3422H
RT port mode control register 3 (8 bits)	RPMC3B	400A 3423H
RT port mode control register 0 (16 bits)	RPMC0H	400A 3420H
RT port mode control register 2 (16 bits)	RPMC2H	400A 3422H
RT port mode control register 0 (32 bits)	RPMC0W	400A 3420H
RT port function control register 0 (8 bits)	RPFC0B	400A 3430H
RT port function control register 1 (8 bits)	RPFC1B	400A 3431H
RT port function control register 2 (8 bits)	RPFC2B	400A 3432H
RT port function control register 3 (8 bits)	RPFC3B	400A 3433H
RT port function control register 0 (16 bits)	RPFC0H	400A 3430H
RT port function control register 2 (16 bits)	RPFC2H	400A 3432H
RT port function control register 0 (32 bits)	RPFC0W	400A 3430H

(5/6)

Register name	Symbol	Address
RT port function control expansion register 0 (8 bits)	RPFCE0B	400A 3440H
RT port function control expansion register 1 (8 bits)	RPFCE1B	400A 3441H
RT port function control expansion register 2 (8 bits)	RPFCE2B	400A 3442H
RT port function control expansion register 3 (8 bits)	RPFCE3B	400A 3443H
RT port function control expansion register 0 (16 bits)	RPFCE0H	400A 3440H
RT port function control expansion register 2 (16 bits)	RPFCE2H	400A 3442H
RT port function control expansion register 0 (32 bits)	RPFCE0W	400A 3440H
RT port pin input register 0 (8 bits)	RPIN0B	400A 3450H
RT port pin input register 1 (8 bits)	RPIN1B	400A 3451H
RT port pin input register 2 (8 bits)	RPIN2B	400A 3452H
RT port pin input register 3 (8 bits)	RPIN3B	400A 3453H
RT port pin input register 0 (16 bits)	RPIN0H	400A 3450H
RT port pin input register 2 (16 bits)	RPIN2H	400A 3452H
RT port pin input register 0 (32 bits)	RPIN0W	400A 3450H

(6/6)

Register name	Symbol	Address
Buffer function change register P0L	DRCTLP0L	4001 0220H
Buffer function change register P0H	DRCTLP0H	4001 0224H
Buffer function change register P1L	DRCTLP1L	4001 0228H
Buffer function change register P1H	DRCTLP1H	4001 022CH
Buffer function change register P2L	DRCTLP2L	4001 0230H
Buffer function change register P2H	DRCTLP2H	4001 0234H
Buffer function change register P3L	DRCTLP3L	4001 0238H
Buffer function change register P3H	DRCTLP3H	4001 023CH
Buffer function change register P4L	DRCTLP4L	4001 0240H
Buffer function change register P4H	DRCTLP4H	4001 0244H
Buffer function change register P5L	DRCTLP5L	4001 0248H
Buffer function change register P5H	DRCTLP5H	4001 024CH
Buffer function change register P6L	DRCTLP6L	4001 0250H
Buffer function change register P6H	DRCTLP6H	4001 0254H
Buffer function change register P7L	DRCTLP7L	4001 0258H
Buffer function change register P7H	DRCTLP7H	4001 025CH
Buffer function change register RP0L	DRCTLRP0L	4001 0260H
Buffer function change register RP0H	DRCTLRP0H	4001 0264H
Buffer function change register RP1L	DRCTLRP1L	4001 0268H
Buffer function change register RP1H	DRCTLRP1H	4001 026CH
Buffer function change register RP2L	DRCTLRP2L	4001 0270H
Buffer function change register RP2H	DRCTLRP2H	4001 0274H
Buffer function change register RP3L	DRCTLRP3L	4001 0278H
Buffer function change register RP3H	DRCTLRP3H	4001 027CH

7.3.1 Port registers (P, RP)

The R-IN32M3-EC incorporates twelve 3-state I/O ports. Input or output mode can be specified in 1-bit units. For output ports, the port register can be used to write the output level. If a port register is read, the value of the output latch is read. Use the PINn or RPINm register to read the pin level.

	7	6	5	4	3	2	1	0	Address	Initial value
P0B	P07	P06	P05	P04	P03	P02	P01	P00	400A 3000H	00H
P1B	P17	P16	P15	P14	P13	P12	P11	P10	400A 3001H	00H
P2B	P27	P26	P25	P24	P23	P22	P21	P20	400A 3002H	00H
P3B	P37	P36	P35	P34	P33	P32	P31	P30	400A 3003H	00H
P4B	P47	P46	P45	P44	P43	P42	P41	P40	400A 3004H	00H
P5B	P57	P56	P55	P54	P53	P52	P51	P50	400A 3005H	00H
P6B	P67	P66	P65	P64	P63	P62	P61	P60	400A 3006H	00H
P7B	P77	P76	P75	P74	P73	P72	P71	P70	400A 3007H	00H
RP0B	RP07	RP06	RP05	RP04	RP03	RP02	RP01	RP00	400A 3400H	00H
RP1B	RP17	RP16	RP15	RP14	RP13	RP12	RP11	RP10	400A 3401H	00H
RP2B	RP27	RP26	RP25	RP24	RP23	RP22	RP21	RP20	400A 3402H	00H
RP3B	RP37	RP36	RP35	RP34	RP33	RP32	RP31	RP30	400A 3403H	00H

Bit position	Bit name	Function
7 to 0	Pmn/RPln	Set the value of the output latch when the port is used in output mode. If read, the value of the output latch is read.

Figure 7.2 Port registers (in 8-bit notation)

Remark l = 0 to 3, m = 0 to 7, n = 0 to 7

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
P0H	P17	P16	P15	P14	P13	P12	P11	P10	P07	P06	P05	P04	P03	P02	P01	P00	Address 400A 3000H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
P2H	P37	P36	P35	P34	P33	P32	P31	P30	P27	P26	P25	P24	P23	P22	P21	P20	Address 400A 3002H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
P4H	P57	P56	P55	P54	P53	P52	P51	P50	P47	P46	P45	P44	P43	P42	P41	P40	Address 400A 3004H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
P6H	P77	P76	P75	P74	P73	P72	P71	P70	P67	P66	P65	P64	P63	P62	P61	P60	Address 400A 3006H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
RP0H	RP17	RP16	RP15	RP14	RP13	RP12	RP11	RP10	RP07	RP06	RP05	RP04	RP03	RP02	RP01	RP00	Address 400A 3400H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
RP2H	RP37	RP36	RP35	RP34	RP33	RP32	RP31	RP30	RP27	RP26	RP25	RP24	RP23	RP22	RP21	RP20	Address 400A 3402H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H

Bit position	Bit name	Function
15 to 0	Pmn/RPln	Set the value of the output latch when the port is used in output mode. If read, the value of the output latch is read.

Figure 7.3 Port registers (in 16-bit notation)

Remark l = 0 to 3, m = 0 to 7, n = 0 to 7

P0W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
P37	P36	P35	P34	P33	P32	P31	P30	P27	P26	P25	P24	P23	P22	P21	P20	P17	P16	P15	P14	P13	P12	P11	P10	P07	P06	P05	P04	P03	P02	P01	P00	400A 3000H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																																0000 0000H

P4W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
P77	P76	P75	P74	P73	P72	P71	P70	P67	P66	P65	P64	P63	P62	P61	P60	P57	P56	P55	P54	P53	P52	P51	P50	P47	P46	P45	P44	P43	P42	P41	P40	400A 3004H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																																0000 0000H

RP0W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RP37	RP36	RP35	RP34	RP33	RP32	RP31	RP30	RP27	RP26	RP25	RP24	RP23	RP22	RP21	RP20	RP17	RP16	RP15	RP14	RP13	RP12	RP11	RP10	RP07	RP06	RP05	RP04	RP03	RP02	RP01	RP00	400A 3400H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																																0000 0000H

Bit position	Bit name	Function
31 to 0	Pmn/RPln	Set the value of the output latch when the port is used in output mode. If read, the value of the output latch is read.

Figure 7.4 Port registers (in 32-bit notation)

Remark l = 0 to 3, m = 0 to 7, n = 0 to 7

7.3.2 Port mode registers (PM, RPM)

These registers are used to set a port to input or output mode.

	7	6	5	4	3	2	1	0	Address	Initial value
PM0B	PM07	PM06	PM05	PM04	PM03	PM02	PM01	PM00	400A 3010H	FFH
PM1B	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10	400A 3011H	FFH
PM2B	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	400A 3012H	FFH
PM3B	PM37	PM36	PM35	PM34	PM33	PM32	PM31	PM30	400A 3013H	FFH
PM4B	PM47	PM46	PM45	PM44	PM43	PM42	PM41	PM40	400A 3014H	FFH
PM5B	PM57	PM56	PM55	PM54	PM53	PM52	PM51	PM50	400A 3015H	FFH
PM6B	PM67	PM66	PM65	PM64	PM63	PM62	PM61	PM60	400A 3016H	FFH
PM7B	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	400A 3017H	FFH
RPM0B	RPM07	RPM06	RPM05	RPM04	RPM03	RPM02	RPM01	RPM00	400A 3410H	FFH
RPM1B	RPM17	RPM16	RPM15	RPM14	RPM13	RPM12	RPM11	RPM10	400A 3411H	FFH
RPM2B	RPM27	RPM26	RPM25	RPM24	RPM23	RPM22	RPM21	RPM20	400A 3412H	FFH
RPM3B	RPM37	RPM36	RPM35	RPM34	RPM33	RPM32	RPM31	RPM30	400A 3413H	FFH

Bit position	Bit name	Function
7 to 0	PMmn/ RPMln	Set the port to input or output mode. 0: Output mode (output buffer is on) 1: Input mode (output buffer is off) (initial value)

Figure 7.5 Port mode registers (in 8-bit notation)

Remark l = 0 to 3, m = 0 to 7, n = 0 to 7

PM0H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10	PM07	PM06	PM05	PM04	PM03	PM02	PM01	PM00	400A 3010H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value FFFFH

PM2H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PM37	PM36	PM35	PM34	PM33	PM32	PM31	PM30	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	400A 3012H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value FFFFH

PM4H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PM57	PM56	PM55	PM54	PM53	PM52	PM51	PM50	PM47	PM46	PM45	PM44	PM43	PM42	PM41	PM40	400A 3014H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value FFFFH

PM6H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	PM67	PM66	PM65	PM64	PM63	PM62	PM61	PM60	400A 3016H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value FFFFH

RPM0H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPM 17	RPM 16	RPM 15	RPM 14	RPM 13	RPM 12	RPM 11	RPM 10	RPM 07	RPM 06	RPM 05	RPM 04	RPM 03	RPM 02	RPM 01	RPM 00	400A 3410H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value FFFFH

RPM2H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPM 37	RPM 36	RPM 35	RPM 34	RPM 33	RPM 32	RPM 31	RPM 30	RPM 27	RPM 26	RPM 25	RPM 24	RPM 23	RPM 22	RPM 21	RPM 20	400A 3412H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value FFFFH

Bit position	Bit name	Function
15 to 0	PMmn/ RPMln	Set the port to input or output mode. 0: Output mode (output buffer is on) 1: Input mode (output buffer is off) (initial value)

Figure 7.6 Port mode registers (in 16-bit notation)

Remark l = 0 to 3, m = 0 to 7, n = 0 to 7

PM0W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PM37	PM36	PM35	PM34	PM33	PM32	PM31	PM30	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10	PM07	PM06	PM05	PM04	PM03	PM02	PM01	PM00	400A 3010H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value: FFFF FFFFH

PM4W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	PM67	PM66	PM65	PM64	PM63	PM62	PM61	PM60	PM57	PM56	PM55	PM54	PM53	PM52	PM51	PM50	PM47	PM46	PM45	PM44	PM43	PM42	PM41	PM40	400A 3014H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value: FFFF FFFFH

RPM0W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPM37	RPM36	RPM35	RPM34	RPM33	RPM32	RPM31	RPM30	RPM27	RPM26	RPM25	RPM24	RPM23	RPM22	RPM21	RPM20	RPM17	RPM16	RPM15	RPM14	RPM13	RPM12	RPM11	RPM10	RPM07	RPM06	RPM05	RPM04	RPM03	RPM02	RPM01	RPM00	400A 3410H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value: FFFF FFFFH

Bit position	Bit name	Function
31 to 0	PMmn/RPMln	Set the port to input or output mode. 0: Output mode (output buffer is on) 1: Input mode (output buffer is off) (initial value)

Figure 7.7 Port mode registers (in 32-bit notation)

Remark l = 0 to 3, m = 0 to 7, n = 0 to 7

7.3.3 Port mode control register (PMC, RPMC)

These registers are used to select whether to use a port as a port or for its alternate function.

	7	6	5	4	3	2	1	0	Address	Initial value
PMC0B	PMC07	PMC06	PMC05	PMC04	PMC03	PMC02	PMC01	PMC00	400A 3020H	00H
PMC1B	PMC17	PMC16	PMC15	PMC14	PMC13	PMC12	PMC11	PMC10	400A 3021H	00H Note
PMC2B	PMC27	PMC26	PMC25	PMC24	PMC23	PMC22	PMC21	PMC20	400A 3022H	00H Note
PMC3B	PMC37	PMC36	PMC35	PMC34	PMC33	PMC32	PMC31	PMC30	400A 3023H	00H Note
PMC4B	PMC47	PMC46	PMC45	PMC44	PMC43	PMC42	PMC41	PMC40	400A 3024H	00H Note
PMC5B	PMC57	PMC56	PMC55	PMC54	PMC53	PMC52	PMC51	PMC50	400A 3025H	00H Note
PMC6B	PMC67	PMC66	PMC65	PMC64	PMC63	PMC62	PMC61	PMC60	400A 3026H	00H Note
PMC7B	PMC77	PMC76	PMC75	PMC74	PMC73	PMC72	PMC71	PMC70	400A 3027H	00H
RPMC0B	RPMC07	RPMC06	RPMC05	RPMC04	RPMC03	RPMC02	RPMC01	RPMC00	400A 3420H	00H Note
RPMC1B	RPMC17	RPMC16	RPMC15	RPMC14	RPMC13	RPMC12	RPMC11	RPMC10	400A 3421H	00H Note
RPMC2B	RPMC27	RPMC26	RPMC25	RPMC24	RPMC23	RPMC22	RPMC21	RPMC20	400A 3422H	00H Note
RPMC3B	RPMC37	RPMC36	RPMC35	RPMC34	RPMC33	RPMC32	RPMC31	RPMC30	400A 3423H	00H Note

Bit position	Bit name	Function
7 to 0	PMCmn/ RPMCln	Specify whether to use the port as a port or for its alternate function. 0: Port mode. (The Inactive level is input to the input pin of the alternate function.) 1: Alternate function (control mode)

Figure 7.8 Port mode control registers (in 8-bit notation)

Note The initial value depends on the pin status. For details, see 2.2 Port status.

Remark l = 0 to 3, m = 0 to 7, n = 0 to 7

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PMC0H	PMC17	PMC16	PMC15	PMC14	PMC13	PMC12	PMC11	PMC10	PMC07	PMC06	PMC05	PMC04	PMC03	PMC02	PMC01	PMC00	400A 3020H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																	0000H[Note]

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PMC2H	PMC37	PMC36	PMC35	PMC34	PMC33	PMC32	PMC31	PMC30	PMC27	PMC26	PMC25	PMC24	PMC23	PMC22	PMC21	PMC20	400A 3022H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																	0000H[Note]

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PMC4H	PMC57	PMC56	PMC55	PMC54	PMC53	PMC52	PMC51	PMC50	PMC47	PMC46	PMC45	PMC44	PMC43	PMC42	PMC41	PMC40	400A 3024H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																	0000H[Note]

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PMC6H	PMC77	PMC76	PMC75	PMC74	PMC73	PMC72	PMC71	PMC70	PMC67	PMC66	PMC65	PMC64	PMC63	PMC62	PMC61	PMC60	400A 3026H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																	0000H[Note]

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPMC0H	RPMC17	RPMC16	RPMC15	RPMC14	RPMC13	RPMC12	RPMC11	RPMC10	RPMC07	RPMC06	RPMC05	RPMC04	RPMC03	RPMC02	RPMC01	RPMC00	400A 3420H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																	0000H[Note]

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPMC2H	RPMC37	RPMC36	RPMC35	RPMC34	RPMC33	RPMC32	RPMC31	RPMC30	RPMC27	RPMC26	RPMC25	RPMC24	RPMC23	RPMC22	RPMC21	RPMC20	400A 3422H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																	0000H[Note]

Bit position	Bit name	Function
15 to 0	PMCmn/ RPMCln	Specify whether to use the port as a port or for its alternate function. 0: Port mode. (The Inactive level is input to the input pin of the alternate function.) 1: Alternate function (control mode)

Figure 7.9 Port mode control registers (in 16-bit notation)

Note The initial value depends on the pin status. For details, see 2.2 Port status.

Remark l = 0 to 3, m = 0 to 7, n = 0 to 7

PMC0W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMC37	PMC36	PMC35	PMC34	PMC33	PMC32	PMC31	PMC30	PMC27	PMC26	PMC25	PMC24	PMC23	PMC22	PMC21	PMC20	PMC17	PMC16	PMC15	PMC14	PMC13	PMC12	PMC11	PMC10	PMC07	PMC06	PMC05	PMC04	PMC03	PMC02	PMC01	PMC00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 400A 3020H
Initial value: 0000 0000H[Note]

PMC4W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMC77	PMC76	PMC75	PMC74	PMC73	PMC72	PMC71	PMC70	PMC67	PMC66	PMC65	PMC64	PMC63	PMC62	PMC61	PMC60	PMC57	PMC56	PMC55	PMC54	PMC53	PMC52	PMC51	PMC50	PMC47	PMC46	PMC45	PMC44	PMC43	PMC42	PMC41	PMC40
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 400A 3024H
Initial value: 0000 0000H[Note]

RPMC0W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RPMC37	RPMC36	RPMC35	RPMC34	RPMC33	RPMC32	RPMC31	RPMC30	RPMC27	RPMC26	RPMC25	RPMC24	RPMC23	RPMC22	RPMC21	RPMC20	RPMC17	RPMC16	RPMC15	RPMC14	RPMC13	RPMC12	RPMC11	RPMC10	RPMC07	RPMC06	RPMC05	RPMC04	RPMC03	RPMC02	RPMC01	RPMC00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 400A 3420H
Initial value: 0000 0000H[Note]

Bit position	Bit name	Function
31 to 0	PMCmn/RPMCln	Specify whether to use the port as a port or for its alternate function. 0: Port mode. (The Inactive level is input to the input pin of the alternate function.) 1: Alternate function (control mode)

Figure 7.10 Port mode control registers (in 32-bit notation)

Note The initial value depends on the pin status. For details, see 2.2 Port status.

Remark l = 0 to 3, m = 0 to 7, n = 0 to 7

7.3.4 Port function control registers (PFC, RPFC)

These registers are used to specify which alternate function is used. These registers can be set in 1-bit units

	7	6	5	4	3	2	1	0	Address	Initial value
PFC0B	PFC07	PFC06	PFC05	PFC04	PFC03	PFC02	0	0	400A 3030H	00H
PFC1B	0	0	0	0	0	PFC12	PFC11	PFC10	400A 3031H	00H
PFC2B	PFC27	PFC26	0	PFC24	0	0	0	0	400A 3032H	00H Note1
PFC3B	PFC37	PFC36	PFC35	PFC34	PFC33	PFC32	0	0	400A 3033H	00H Note1
PFC4B	PFC47	PFC46	PFC45	PFC44	PFC43	PFC42	PFC41	PFC40	400A 3034H	00H Note1
PFC5B	PFC57	0	0	PFC54	PFC53	PFC52	0	0	400A 3035H	00H Note1
PFC6B	0	0	0	0	0	0	0	0	400A 3036H	00H
PFC7B	0	0	0	0	0	0	0	0	400A 3037H	00H
RPFC0B	RPFC07	RPFC06	0	0	0	0	RPFC01	RPFC00	400A 3430H	00H
RPFC1B	0	0	0	0	0	0	0	0	400A 3431H	00H
RPFC2B	RPFC27	RPFC26	RPFC25	RPFC24	0	0	0	RPFC20	400A 3432H	00H
RPFC3B	0	0	0	0	0	0	0	0	400A 3433H	00H

Bit position	Bit name	Function
7 to 0	PFCmn/ RPFCmn	Specify whether to use alternate functions 1 and 3 or alternate functions 2 and 4. 0: Alternate function 1 Note 2/Alternate function 3 Note 3 1: Alternate function 2 Note 2/Alternate function 4 Note 3

Figure 7.11 Port function control registers (in 8-bit notation)

Notes 1. The initial value depends on the pin status. For details, see 2.2 Port status.

2. To use alternate function 1 or 2, the bit corresponding to the function in the PFCE/RPFCE register must be set to 0.

3. To use alternate function 3 or 4, the bit corresponding to the function in the PFCE/RPFCE register must be set to 1.

Remark l = 0 to 3, m = 0 to 7, n = 0 to 7

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFC0H	0	0	0	0	0	PFC12	PFC11	PFC10	PFC07	PFC06	PFC05	PFC04	PFC03	PFC02	0	0	400A 3030H
	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	0	Initial value 0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFC2H	PFC37	PFC36	PFC35	PFC34	PFC33	PFC32	0	0	PFC27	PFC26	0	PFC24	0	0	0	0	400A 3032H
	R/W	R/W	R/W	R/W	R/W	R/W	0	0	R/W	R/W	0	R/W	0	0	0	0	Initial value 0000H[Note 1]

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFC4H	PFC57	0	0	PFC54	PFC53	PFC52	0	0	PFC47	PFC46	PFC45	PFC44	PFC43	PFC42	PFC41	PFC40	400A 3034H
	R/W	0	0	R/W	R/W	R/W	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H[Note 1]

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFC6H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	400A 3036H
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Initial value 0000H[Note 1]

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPFC0H	0	0	0	0	0	0	0	0	RPFC07	RPFC06	0	0	0	0	RPFC01	RPFC00	400A 3430H
	0	0	0	0	0	0	0	0	R/W	R/W	0	0	0	0	R/W	R/W	Initial value 0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPFC2H	0	0	0	0	0	0	0	0	RPFC27	RPFC26	RPFC25	RPFC24	0	0	0	RPFC20	400A 3432H
	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	0	0	0	R/W	Initial value 0000H

Bit position	Bit name	Function
15-0	PFCmn / RPFCmn	Specify whether to use alternate functions 1 and 3 or alternate functions 2 and 4. 0: Alternate function 1[Note 2]/Alternate function 3[Note 3] 1: Alternate function 2[Note 2]/Alternate function 4[Note 3]

Figure 7.12 Port function control registers (in 16-bit notation)

Notes 1. The initial value depends on the pin status. For details, see 2.2 Port status.

2. To use alternate function 1 or 2, the bit corresponding to the function in the PFCE/RPFCE register must be set to 0.

3. To use alternate function 3 or 4, the bit corresponding to the function in the PFCE/RPFCE register must be set to 1.

Remark l = 0 to 3, m = 0 to 7, n = 0 to 7

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFC0W	PFC37	PFC36	PFC35	PFC34	PFC33	PFC32	0	0	PFC27	PFC26	0	PFC24	0	0	0	0	0	0	0	0	0	PFC12	PFC11	PFC10	PFC07	PFC06	PFC05	PFC04	PFC03	PFC02	0	0	400A 3030H Initial value 0000 0000H[Note]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	0	R/W	R/W	0	R/W	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	0	
PFC4W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PFC57	0	0	PFC54	PFC53	PFC52	0	0	PFC47	PFC46	PFC45	PFC44	PFC43	PFC42	PFC41	PFC40	400A 3034H Initial value 0000 0000H[Note]
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	0	0	R/W	R/W	R/W	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
RPFC0W	0	0	0	0	0	0	0	0	RPFC27	RPFC26	RPFC25	RPFC24	0	0	0	RPFC20	0	0	0	0	0	0	0	0	RPFC07	RPFC06	0	0	0	0	RPFC01	RPFC00	400A 3430H Initial value 0000 0000H[Note]
R/W	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	0	0	0	R/W	0	0	0	0	0	0	0	0	R/W	R/W	0	0	0	0	R/W	R/W	

Bit position	Bit name	Function
31-0	PFCmn / RPFCln	Specify whether to use alternate functions 1 and 3 or alternate functions 2 and 4. 0: Alternate function 1Note 2/Alternate function 3Note 3 1: Alternate function 2Note 2/Alternate function 4Note 3

Figure 7.13 Port function control registers (in 32-bit notation)

Notes 1. The initial value depends on the pin status. For details, see 2.2 Port status.

2. To use alternate function 1 or 2, the bit corresponding to the function in the PFCE/RPFCE register must be set to 0.

3. To use alternate function 3 or 4, the bit corresponding to the function in the PFCE/RPFCE register must be set to 1.

Remark l = 0 to 3, m = 0 to 7, n = 0 to 7

7.3.5 Port function control expansion registers (PFCE, RPFCE)

These registers are used to specify which alternate expansion function is used. These registers can be set in 1-bit units.

	7	6	5	4	3	2	1	0	Address	Initial value
PFCE0B	PFCE07	PFCE06	PFCE05	PFCE04	PFCE03	PFCE02	0	PFCE00	400A 3040H	00H
PFCE1B	0	0	0	0	PFCE13	PFCE12	1	1	400A 3041H	00H
PFCE2B	0	PFCE26	PFCE25	PFCE24	PFCE23	PFCE22	PFCE21	PFCE20	400A 3042H	00H
PFCE3B	PFCE37	PFCE36	PFCE35	PFCE34	PFCE33	PFCE32	0	0	400A 3043H	00H[1]
PFCE4B	0	0	0	0	0	PFCE42	0	0	400A 3044H	00H Note 1
PFCE5B	PFCE57	PFCE56	0	PFCE54	PFCE53	PFCE52	PFCE51	PFCE50	400A 3045H	00H
PFCE6B	0	PFCE66	PFCE65	PFCE64	PFCE63	PFCE62	0	0	400A 3046H	00H
PFCE7B	PFCE77	PFCE76	PFCE75	PFCE74	PFCE73	PFCE72	PFCE71	PFCE70	400A 3047H	00H
RPFCE0B	0	0	RPFCE05	RPFCE04	RPFCE03	RPFCE02	RPFCE01	RPFCE00	400A 3440H	00H Note 1
RPFCE1B	0	0	0	0	0	0	0	0	400A 3441H	00H
RPFCE2B	0	0	0	0	0	0	0	0	400A 3442H	00H
RPFCE3B	0	0	0	0	0	0	0	0	400A 3443H	00H

Bit position	Bit name	Function
7 to 0	PFCEmn/ RPFCEln	Specify whether to use alternate functions 1 and 2 or alternate functions 3 and 4. 0: Alternate function 1 Note 2/Alternate function 2 Note 3 1: Alternate function 3 Note 2/Alternate function 4 Note 3

Figure 7.13 Port function control expansion registers (in 8-bit notation)

Notes 1. The initial value depends on the pin status. For details, see 2.2 Port status.

2. To use alternate function 1 or 3, the bit corresponding to the function in the PFC/RPFC register must be set to 0.

3. To use alternate function 2 or 4, the bit corresponding to the function in the PFC/RPFC register must be set to 1.

Remark l = 0 to 3, m = 0 to 7, n = 0 to 7

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFCE0H	0	0	0	0	PFCE13	PFCE12	1	1	PFCE07	PFCE06	PFCE05	PFCE04	PFCE03	PFCE02	0	PFCE00	400A 3040H
	0	0	0	0	R/W	R/W	1	1	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFCE2H	PFCE37	PFCE36	PFCE35	PFCE34	PFCE33	PFCE32	0	0	0	PFCE26	PFCE25	PFCE24	PFCE23	PFCE22	PFCE21	PFCE20	400A 3042H
	R/W	R/W	R/W	R/W	R/W	R/W	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H Note 1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFCE4H	PFCE57	PFCE56	0	PFCE54	PFCE53	PFCE52	PFCE51	PFCE50	0	0	0	0	0	PFCE42	0	0	400A 3044H
	R/W	R/W	0	R/W	R/W	R/W	R/W	R/W	0	0	0	0	0	R/W	0	0	Initial value 0000H Note 1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFCE6H	PFCE77	PFCE76	PFCE75	PFCE74	PFCE73	PFCE72	PFCE71	PFCE70	0	PFCE66	PFCE65	PFCE64	PFCE63	PFCE62	0	0	400A 3046H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	R/W	R/W	R/W	R/W	R/W	0	0	Initial value 0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPFCE0H	0	0	0	0	0	0	0	0	0	0	RPFCE05	RPFCE04	RPFCE03	RPFCE02	RPFCE01	RPFCE00	400A 3440H
	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H Note 1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPFCE2H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	400A 3442H
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Initial value 0000H

Bit position	Bit name	Function
15 to 0	PFCEmn/ RPFCEln	Specify whether to use alternate functions 1 and 2 or alternate functions 3 and 4. 0: Alternate function 1Note 2/Alternate function 2Note 3 1: Alternate function 3Note 2/Alternate function 4Note 3

Figure 7.14 Port function control expansion registers (in 16-bit notation)

Notes 1. The initial value depends on the pin status. For details, see 2.2 Port status.

2. To use alternate function 1 or 3, the bit corresponding to the function in the PFC/RPFC register must be set to 0.

3. To use alternate function 2 or 4, the bit corresponding to the function in the PFC/RPFC register must be set to 1.

Remark l = 0 to 3, m = 0 to 7, n = 0 to 7

PFCE0W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PFCE37	PFCE36	PFCE35	PFCE34	PFCE33	PFCE32	0	0	0	PFCE26	PFCE25	PFCE24	PFCE23	PFCE22	PFCE21	PFCE20	0	0	0	0	PFCE13	PFCE12	1	1	PFCE07	PFCE06	PFCE05	PFCE04	PFCE03	PFCE02	0	PFCE00
R/W	R/W	R/W	R/W	R/W	R/W	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	0	0	0	R/W	R/W	1	1	R/W	R/W	R/W	R/W	R/W	R/W	0	R/W

Address: 400A 3040H
Initial value: 0000 0000H Note 1

PFCE4W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PFCE77	PFCE76	PFCE75	PFCE74	PFCE73	PFCE72	PFCE71	PFCE70	0	PFCE66	PFCE65	PFCE64	PFCE63	PFCE62	0	0	PFCE57	PFCE56	0	PFCE54	PFCE53	PFCE52	PFCE51	PFCE50	0	0	0	0	0	PFCE42	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	R/W	R/W	R/W	R/W	R/W	0	0	R/W	R/W	0	R/W	R/W	R/W	R/W	R/W	0	0	0	0	0	R/W	0	0

Address: 400A 3044H
Initial value: 0000 0000H Note 1

RPFCE0W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RPFCE05	RPFCE04	RPFCE03	RPFCE02	RPFCE01	RPFCE00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W

Address: 400A 3440H
Initial value: 0000 0000H Note 1

Bit position	Bit name	Function
31 to 0	PFCEmn/ RPFCEln	Specify whether to use alternate functions 1 and 2 or alternate functions 3 and 4. 0: Alternate function 1 Note 2/Alternate function 2 Note 3 1: Alternate function 3 Note 2/Alternate function 4 Note 3

Figure 7.15 Port function control expansion registers (in 32-bit notation)

Notes 1. The initial value depends on the pin status. For details, see 2.2 Port status.

2. To use alternate function 1 or 3, the bit corresponding to the function in the PFC/RPFC register must be set to 0.

3. To use alternate function 2 or 4, the bit corresponding to the function in the PFC/RPFC register must be set to 1.

Remark l = 0 to 3, m = 0 to 7, n = 0 to 7

7.3.6 Port pin input registers (PIN, RPIN)

These are read-only registers for reading the input level of port pins.

	7	6	5	4	3	2	1	0	Address	Initial value
PIN0B	PIN07	PIN06	PIN05	PIN04	PIN03	PIN02	PIN01	PIN00	400A 3050H	Undefined
PIN1B	PIN17	PIN16	PIN15	PIN14	PIN13	PIN12	PIN11	PIN10	400A 3051H	Undefined
PIN2B	PIN27	PIN26	PIN25	PIN24	PIN23	PIN22	PIN21	PIN20	400A 3052H	Undefined
PIN3B	PIN37	PIN36	PIN35	PIN34	PIN33	PIN32	PIN31	PIN30	400A 3053H	Undefined
PIN4B	PIN47	PIN46	PIN45	PIN44	PIN43	PIN42	PIN41	PIN40	400A 3054H	Undefined
PIN5B	PIN57	PIN56	PIN55	PIN54	PIN53	PIN52	PIN51	PIN50	400A 3055H	Undefined
PIN6B	PIN67	PIN66	PIN65	PIN64	PIN63	PIN62	PIN61	PIN60	400A 3056H	Undefined
PIN7B	PIN77	PIN76	PIN75	PIN74	PIN73	PIN72	PIN71	PIN70	400A 3057H	Undefined
RPIN0B	RPIN07	RPIN06	RPIN05	RPIN04	RPIN03	RPIN02	RPIN01	RPIN00	400A 3450H	Undefined
RPIN1B	RPIN17	RPIN16	RPIN15	RPIN14	RPIN13	RPIN12	RPIN11	RPIN10	400A 3451H	Undefined
RPIN2B	RPIN27	RPIN26	RPIN25	RPIN24	RPIN23	RPIN22	RPIN21	RPIN20	400A 3452H	Undefined
RPIN3B	RPIN37	RPIN36	RPIN35	RPIN34	RPIN33	RPIN32	RPIN31	RPIN30	400A 3453H	Undefined

Bit position	Bit name	Function
7 to 0	PINmn/ RPINln	Use to read the input level of the port pin.

Figure 7.16 Port pin input registers (in 8-bit notation)

Remark l = 0 to 3, m = 0 to 7, n = 0 to 7

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PIN0H	PIN 17	PIN 16	PIN 15	PIN 14	PIN 13	PIN 12	PIN 11	PIN 10	PIN 07	PIN 06	PIN 05	PIN 04	PIN 03	PIN 02	PIN 01	PIN 00	400A 3050H
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial value
																	Undefined

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PIN2H	PIN 37	PIN 36	PIN 35	PIN 34	PIN 33	PIN 32	PIN 31	PIN 30	PIN 27	PIN 26	PIN 25	PIN 24	PIN 23	PIN 22	PIN 21	PIN 20	400A 3052H
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial value
																	Undefined

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PIN4H	PIN 57	PIN 56	PIN 55	PIN 54	PIN 53	PIN 52	PIN 51	PIN 50	PIN 47	PIN 46	PIN 45	PIN 44	PIN 43	PIN 42	PIN 41	PIN 40	400A 3054H
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial value
																	Undefined

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PIN6H	PIN 77	PIN 76	PIN 75	PIN 74	PIN 73	PIN 72	PIN 71	PIN 70	PIN 67	PIN 66	PIN 65	PIN 64	PIN 63	PIN 62	PIN 61	PIN 60	400A 3056H
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial value
																	Undefined

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPIN0H	RPIN 17	RPIN 16	RPIN 15	RPIN 14	RPIN 13	RPIN 12	RPIN 11	RPIN 10	RPIN 07	RPIN 06	RPIN 05	RPIN 04	RPIN 03	RPIN 02	RPIN 01	RPIN0 0	400A 3450H
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial value
																	Undefined

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPIN2H	RPIN 37	RPIN 36	RPIN 35	RPIN 34	RPIN 33	RPIN 32	RPIN 31	RPIN 30	RPIN 27	RPIN 26	RPIN 25	RPIN 24	RPIN 23	RPIN 22	RPIN 21	RPIN2 0	400A 3452H
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial value
																	Undefined

Bit position	Bit name	Function
15 to 0	PINmn/ RPINln	Use to read the input level of the port pin.

Figure 7.17 Port pin input registers (in 16-bit notation)

Remark l = 0 to 3, m = 0 to 7, n = 0 to 7

PIN0W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PIN37	PIN36	PIN35	PIN34	PIN33	PIN32	PIN31	PIN30	PIN27	PIN26	PIN25	PIN24	PIN23	PIN22	PIN21	PIN20	PIN17	PIN16	PIN15	PIN14	PIN13	PIN12	PIN11	PIN10	PIN07	PIN06	PIN05	PIN04	PIN03	PIN02	PIN01	PIN00
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address: 400A 3050H
Initial value: Undefined

PIN4W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PIN77	PIN76	PIN75	PIN74	PIN73	PIN72	PIN71	PIN70	PIN67	PIN66	PIN65	PIN64	PIN63	PIN62	PIN61	PIN60	PIN57	PIN56	PIN55	PIN54	PIN53	PIN52	PIN51	PIN50	PIN47	PIN46	PIN45	PIN44	PIN43	PIN42	PIN41	PIN40
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address: 400A 3054H
Initial value: Undefined

RPIN0W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RPIN37	RPIN36	RPIN35	RPIN34	RPIN33	RPIN32	RPIN31	RPIN30	RPIN27	RPIN26	RPIN25	RPIN24	RPIN23	RPIN22	RPIN21	RPIN20	RPIN17	RPIN16	RPIN15	RPIN14	RPIN13	RPIN12	RPIN11	RPIN10	RPIN07	RPIN06	RPIN05	RPIN04	RPIN03	RPIN02	RPIN01	RPIN00
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address: 400A 3450H
Initial value: Undefined

Bit position	Bit name	Function
31 to 0	PINmn/RPINln	Use to read the input level of the port pin.

Remark l = 0 to 3, m = 0 to 7, n = 0 to 7

7.4 Available combinations of alternate functions

The combinations of alternate functions that can be specified by using the port-related registers are shown below.

(1) Ports (P00 to P77)

(1/3)

Pin name	PMCmn = 0 (port mode)		PMCmn = 1 (control mode)			
			PFCEmn = 0		PFCEmn = 1	
	PMmn = 0 (output port)	PMmn = 1 (input port)	PFCmn = 0	PFCmn = 1	PFCmn = 0	PFCmn = 1
P00	P00 (output mode)	P00 (input mode)	INTPZ0	-	CCI_RUNLEDZ	-
P01	P01 (output mode)	P01 (input mode)	INTPZ1	-	-	-
P02	P02 (output mode)	P02 (input mode)	INTPZ2	-	CCI_DLINKLEDZ	-
P03	P03 (output mode)	P03 (input mode)	INTPZ3	-	CCI_ERRLEDZ	CCS_MON5
P04	P04 (output mode)	P04 (input mode)	INTPZ4	-	CCI_LERR1LEDZ	CCS_MON6
P05	P05 (output mode)	P05 (input mode)	INTPZ5	-	CCI_LERR2LEDZ	CCS_MON7
P06	P06 (output mode)	P06 (input mode)	PHYLINK0	-	CCI_SDLEDZ	CCS_MON0
P07	P07 (output mode)	P07 (input mode)	PHYLINK1	-	CCIRDLEDZ	CCS_RESOUT
P10	P10 (output mode)	P10 (input mode)	-	-	-	CCS_REFSTB
P11	P11 (output mode)	P11 (input mode)	-	-	-	CCS_MON4
P12	P12 (output mode)	P12 (input mode)	INTPZ6	-	CCI_NMIZ	-
P13	P13 (output mode)	P13 (input mode)	INTPZ7	-	CCI_WDTIZ / CCS_WDTZ / CCM_WDTENZ	-
P14	P14 (output mode)	P14 (input mode)	SMSCK	-	-	-
P15	P15 (output mode)	P15 (input mode)	SMSI	-	-	-
P16	P16 (output mode)	P16 (input mode)	SMSO	-	-	-
P17	P17 (output mode)	P17 (input mode)	SMCSZ	-	-	-
P20	P20 (output mode)	P20 (input mode)	RXD0	−	CCM_LINKERRZ	-
P21	P21 (output mode)	P21 (input mode)	TXD0	−	CCM_ERRZ	-
P22	P22 (output mode)	P22 (input mode)	INTPZ8	−	CCS_IOTENSU	-
P23	P23 (output mode)	P23 (input mode)	INTPZ9	−	CCS_SENYU0	-
P24	P24 (output mode)	P24 (input mode)	INTPZ10	ETHSWSECOUT	CCS_SENYU1	-
P25	P25 (output mode)	P25 (input mode)	WDTOUTZ	−	CCS_ERRZ	-
P26	P26 (output mode)	P26 (input mode)	TIN1	TOUT1	CCM_RUNZ / CCS_RUNZ	-
P27	P27 (output mode)	P27 (input mode)	TIN0	TOUT0	-	-

Remark m = 0 to 7, n = 0 to 7

(2/3)

Pin name	PMCmn = 0 (port mode)		PMCmn = 1 (control mode)			
			PFCEmn = 0		PFCEmn = 1	
	PMmn = 0 (output port)	PMmn = 1 (input port)	PFCmn = 0	PFCmn = 1	PFCmn = 0	PFCmn = 1
P30	P30 (output mode)	P30 (input mode)	RXD1	-	-	-
P31	P31 (output mode)	P31 (input mode)	TXD1	-	-	-
P32	P32 (output mode)	P32 (input mode)	DMAREQZ1	-	-	CCS_MON1
P33	P33 (output mode)	P33 (input mode)	DMAACKZ1	CCI_ WAITEDGEH	-	CCS_MON2
P34	P34 (output mode)	P34 (input mode)	DMATCZ1	CCI_WRLENH	-	CCS_MON3
P35	P35 (output mode)	P35 (input mode)	CSISCK1	INTPZ22	CCM_IRZ	-
P36	P36 (output mode)	P36 (input mode)	CSISI1	INTPZ23	CCS_FUSEZ	-
P37	P37 (output mode)	P37 (input mode)	CSISO1	INTPZ24	CCM_MSTZ	-
P40	P40 (output mode)	P40 (input mode)	A1	HA1	-	-
P41	P41 (output mode)	P41 (input mode)	WAITZ	HWAITZ	-	-
P42	P42 (output mode)	P42 (input mode)	SLEEPING	HERROUTZ	CCM_SDGCZ	-
P43	P43 (output mode)	P43 (input mode)	INTPZ11	HBUSCLK	-	-
P44	P44 (output mode)	P44 (input mode)	CSZ1	HPGCSZ	-	-
P45	P45 (output mode)	P45 (input mode)	CSISCK0	WAITZ1	-	-
P46	P46 (output mode)	P46 (input mode)	CSISI0	WAITZ2	-	-
P47	P47 (output mode)	P47 (input mode)	CSISO0	WAITZ3	-	-
P50	P50 (output mode)	P50 (input mode)	CSZ3	-	CCM_LNKRUNZ / CCS_LNKRUNZ	-
P51	P51 (output mode)	P51 (input mode)	CSZ2	-	CCM_RDLEDZ / CCS_RDLEDZ	-
P52	P52 (output mode)	P52 (input mode)	TIN3	TOUT3	CCS_SDGATEON	-
P53	P53 (output mode)	P53 (input mode)	CRXD0	CCS_RD	CCM_RD	-
P54	P54 (output mode)	P54 (input mode)	CTXD0	CCS_SD	CCM_SD	-
P55	P55 (output mode)	P55 (input mode)	CRXD1	–	–	-
P56	P56 (output mode)	P56 (input mode)	CTXD1	-	CCI_PHYREZ1	-
P57	P57 (output mode)	P57 (input mode)	TIN2	TOUT2	CCI_PHYREZ0	-

Remark m = 0 to 7, n = 0 to 7

(3/3)

Pin name	PMCmn = 0 (port mode)		PMCmn = 1 (control mode)			
			PFCEmn = 0		PFCEmn = 1	
	PMmn = 0 (output port)	PMmn = 1 (input port)	PFCmn = 0	PFCmn = 1	PFCmn = 0	PFCmn = 1
P60	P60 (output mode)	P60 (input mode)	SCL0	–	–	–
P61	P61 (output mode)	P61 (input mode)	SDA0	–	–	–
P62	P62 (output mode)	P62 (input mode)	RTDMAREQZ	–	CCM_MDIN0	–
P63	P63 (output mode)	P63 (input mode)	RTDMAACKZ	–	CCM_MDIN1	–
P64	P64 (output mode)	P64 (input mode)	RTDMATCZ	–	CCM_MDIN2	–
P65	P65 (output mode)	P65 (input mode)	DMAREQZ0	–	CCM_MDIN3	–
P66	P66 (output mode)	P66 (input mode)	DMAACKZ0	–	CCI_INTZ	–
P67	P67 (output mode)	P67 (input mode)	DMATCZ0	–	–	–
P70	P70 (output mode)	P70 (input mode)	CSICS00	–	CCS_STATION_NO_0 / CCM_SNIN0	–
P71	P71 (output mode)	P71 (input mode)	CSICS01	–	CCS_STATION_NO_1 / CCM_SNIN1	–
P72	P72 (output mode)	P72 (input mode)	CSICS10	–	CCS_STATION_NO_2 / CCM_SNIN2	–
P73	P73 (output mode)	P73 (input mode)	CSICS11	–	CCS_STATION_NO_3 / CCM_SNIN3	–
P74	P74 (output mode)	P74 (input mode)	INTPZ12	–	CCS_STATION_NO_4 / CCM_SNIN4	–
P75	P75 (output mode)	P75 (input mode)	INTPZ13	–	CCS_STATION_NO_5 / CCM_SNIN5	–
P76	P76 (output mode)	P76 (input mode)	INTPZ14	–	CCS_STATION_NO_6 / CCM_SNIN6	–
P77	P77 (output mode)	P77 (input mode)	INTPZ15	–	CCS_STATION_NO_7 / CCM_SNIN7	–

Remark m = 0 to 7, n = 0 to 7

(2) Real-time control ports (RP00 to RP37)

Pin name	PMCmn = 0 (port mode)		PMCmn = 1 (control mode)			
			RPFCEmn = 0		RPFCEmn = 1	
	PMmn = 0 (output port)	PMmn = 1 (input port)	RPFCmn = 0	RPFCmn = 1	RPFCmn = 0	RPFCmn = 1
RP00	RP00 (output mode)	RP00 (input mode)	INTPZ16	SCL1	CCM_SDLEDZ / CCS_SDLEDZ	-
RP01	RP01 (output mode)	RP01 (input mode)	INTPZ17	SDA1	CCM_SMSTZ	-
RP02	RP02 (output mode)	RP02 (input mode)	INTPZ18	–	CCS_BS1	-
RP03	RP03 (output mode)	RP03 (input mode)	INTPZ19	–	CCS_BS2	-
RP04	RP04 (output mode)	RP04 (input mode)	INTPZ20	–	CCS_BS4	-
RP05	RP05 (output mode)	RP05 (input mode)	INTPZ21	–	CCS_BS8	-
RP06	RP06 (output mode)	RP06 (input mode)	WRZ2	HWRZ2	-	–
RP07	RP07 (output mode)	RP07 (input mode)	WRZ3	HWRZ3	-	–
RP10	RP10 (output mode)	RP10 (input mode)	D24/HD24	–	-	–
RP11	RP11 (output mode)	RP11 (input mode)	D25/HD25	–	-	–
RP12	RP12 (output mode)	RP12 (input mode)	D26/HD26	–	-	–
RP13	RP13 (output mode)	RP13 (input mode)	D27/HD27	–	-	–
RP14	RP14 (output mode)	RP14 (input mode)	D28/HD28	–	-	–
RP15	RP15 (output mode)	RP15 (input mode)	D29/HD29	–	-	–
RP16	RP16 (output mode)	RP16 (input mode)	D30/HD30	–	-	–
RP17	RP17 (output mode)	RP17 (input mode)	D31/HD31	–	-	-
RP20	RP20 (output mode)	RP20 (input mode)	BCYSTZ	HBCYSTZ	-	-
RP21	RP21 (output mode)	RP21 (input mode)	A21	–	-	-
RP22	RP22 (output mode)	RP22 (input mode)	A22	–	–	-
RP23	RP23 (output mode)	RP23 (input mode)	A23	–	–	-
RP24	RP24 (output mode)	RP24 (input mode)	A24	INTPZ25	–	-
RP25	RP25 (output mode)	RP25 (input mode)	A25	INTPZ26	–	-
RP26	RP26 (output mode)	RP26 (input mode)	A26	INTPZ27	–	-
RP27	RP27 (output mode)	RP27 (input mode)	A27	INTPZ28	–	-
RP30	RP30 (output mode)	RP30 (input mode)	D16/HD16	-	–	-
RP31	RP31 (output mode)	RP31 (input mode)	D17/HD17	-	–	-
RP32	RP32 (output mode)	RP32 (input mode)	D18/HD18	-	–	-
RP33	RP33 (output mode)	RP33 (input mode)	D19/HD19	-	–	-
RP34	RP34 (output mode)	RP34 (input mode)	D20/HD20	-	–	-
RP35	RP35 (output mode)	RP35 (input mode)	D21/HD21	-	–	-
RP36	RP36 (output mode)	RP36 (input mode)	D22/HD22	-	–	-
RP37	RP37 (output mode)	RP37 (input mode)	D23/HD23	-	–	-

Remark m = 0 to 3, n = 0 to 7

7.5 Buffer function change registers (DRCTLP)

For some port pins, the driving capability and whether to connect a pull-up or pull-down resistor can be specified individually.

Set up the DRCTLP registers during initialization after the reset period ends. After that, the setting of each DRCTLP register can only be changed when the corresponding buffer function change pin is not being used. For example, a DRCTLP register setting can be changed at times when only a memory space is being accessed internally.

The DRCTLP register setting becomes valid regardless of the operating mode of the pin (port mode, or control mode in which an alternate function is used).

- Access These registers can be read and written in 32-bit or 16-bit units.

Cautions 1. These registers are write-protected and can only be written after being protection-unlocked by using a special instruction sequence initiated by using the system protection command register (SYSPCMD). For how to unlock protection, see the description of the system protection command register (SYSPCMD). No special instruction sequence is required for reading these registers.

2. Changing the pull-up/pull-down resistor setting affects the level when a pin enters a high-impedance state.

7.5.1 Port 0 buffer function change registers (DRCTLP0L, DRCTLP0H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP0L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP03	PDIOP03	IOLP031	IOLP030	PUIOP02	PDIOP02	IOLP021	IOLP020	PUIOP01	PDIOP01	IOLP011	IOLP010	PUIOP00	PDIOP00	IOLP001	IOLP000	BASE+0220H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0000 9999H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP0H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP07	PDIOP07	IOLP071	IOLP070	PUIOP06	PDIOP06	IOLP061	IOLP060	PUIOP05	PDIOP05	IOLP051	IOLP050	PUIOP04	PDIOP04	IOLP041	IOLP040	BASE+0224H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0000 9999H

Bit position	Bit name	Function
31 to 16	–	Reserved. (Be sure to write 0 to these bits. If read, 0 is returned.)
15,14,11, 10,7,6,3.2	PUIOP0n, PDIOP0n	Specify whether to connect a pull-up or pull-down resistor to the P07 to P00 pins.
13,12,9,8 5,4,1,0	IOLP0n1, IOLP0n0	Specify the driving capability of the P07 to P00 pins.

PUIO	PDIO	Connection of a pull-up or pull-down resistor to the P07 to P00 pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1:	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

IOL1	IOL0	Driving capability of P07 to P00 pins
0	1	6 mA (recommended)
1	1	12 mA
Other than above		Setting prohibited

Remark n = 7 to 0

7.5.2 Port 1 Buffer function change register (DRCTLP1L, DRCTLP1H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP1L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP13	PDIOP13	0	1	PUIOP12	PDIOP12	0	1	PUIOP11	PDIOP11	0	1	PUIOP10	PDIOP10	IOLP101	IOLP100	BASE+0228H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	R/W	R/W	0000 9959H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP1H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP17	PDIOP17	0	1	PUIOP16	PDIOP16	0	1	PUIOP15	PDIOP15	0	1	PUIOP14	PDIOP14	0	1	BASE+022CH
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	0000 9999H

Bit position	Bit name	Function
31 to 16	–	Reserved. (Be sure to write 0 to these bits. If read, 0 is returned.)
15, 14, 11, 10, 7, 6, 3. 2	PUIOP1n, PDIOP1n	Specify whether to connect a pull-up or pull-down resistor to the P17 to P10 pins.

PUIO	PDIO	Connection of a pull-up or pull-down resistor to the P17 to P10 pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1:	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

1, 0	IOLP101, IOLP100	Specify the driving capability of the P10 pin.

IOL1	IOL0	Driving capability of P10 pin
0	1	6 mA (recommended)
1	1	12 mA
Other than above		Setting prohibited

Remark n = 7 to 0

7.5.3 Port 2 Buffer function change register (DRCTLP2L, DRCTLP2H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP2L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP23	PDIOP23	0	1	PUIOP22	PDIOP22	0	1	PUIOP21	PDIOP21	IOLP211	IOLP210	PUIOP20	PDIOP20	IOLP201	IOLP200	BASE+0230H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0000 9999H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP2H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP27	PDIOP27	0	1	PUIOP26	PDIOP26	IOLP261	IOLP260	PUIOP25	PDIOP25	IOLP251	IOLP250	PUIOP24	PDIOP24	0	1	BASE+0234H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	1	0000 9999H

Bit position	Bit name	Function
31 to 16	–	Reserved. (Be sure to write 0 to these bits. If read, 0 is returned.)
15, 14, 11, 10, 7, 6, 3. 2	PUIOP1n, PDIOP1n	Specify whether to connect a pull-up or pull-down resistor to the P27 to P20 pins.

PUIO	PDIO	Connection of a pull-up or pull-down resistor to the P27 to P20 pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1:	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

9,8 5,4,1,0	IOLP2n1, IOLP2n0	Specify the driving capability of the P26 to P24 and P21 and P20 pins

IOL1	IOL0	Driving capability of P26 to P24 and P21 and P20 pins
0	1	6 mA (recommended)
1	1	12 mA
Other than above		Setting prohibited

Remark n = 7 to 0

7.5.4 Port 3 Buffer function change register (DRCTLP3L, DRCTLP3H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP3L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP33	PDIOP33	0	1	PUIOP32	PDIOP32	0	1	PUIOP31	PDIOP31	0	1	PUIOP30	PDIOP30	0	1	BASE+0238H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	0000 9999H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP3H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP37	PDIOP37	IOLP371	IOLP370	PUIOP36	PDIOP36	0	1	PUIOP35	PDIOP35	0	1	PUIOP34	PDIOP34	0	1	BASE+023CH
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	0000 9999H

Bit position	Bit name	Function
31 to 16	–	Reserved. (Be sure to write 0 to these bits. If read, 0 is returned.)
15, 14, 11, 10, 7, 6, 3, 2	PUIOP3n, PDIOP3n	Specify whether to connect a pull-up or pull-down resistor to the P37 to P30 pins.

PUIO	PDIO	Connection of a pull-up or pull-down resistor to the P37 to P30 pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

13, 12	IOLP371, IOLP370	Specify the driving capability of the P37 pin.

IOL1	IOL0	Driving capability of P37 pin
0	1	6 mA (recommended)
1	1	12 mA
Other than above		Setting prohibited

Remark n = 7 to 0

7.5.5 Port 4 Buffer function change register (DRCTLP4L, DRCTLP4H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP4L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP43	PDIOP43	0	1	PUIOP42	PDIOP42	0	1	PUIOP41	PDIOP41	0	1	PUIOP40	PDIOP40	0	1	BASE+0240H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	Initial value 0000 9999H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP4H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP47	PDIOP47	0	1	PUIOP46	PDIOP46	0	1	PUIOP45	PDIOP45	0	1	PUIOP44	PDIOP44	0	1	BASE+0244H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	Initial value 0000 9999H

Bit position	Bit name	Function
31 to 16	–	Reserved. (Be sure to write 0 to these bits. If read, 0 is returned.)
15, 14, 11, 10, 7, 6, 3, 2	PUIOP4n, PDIOP4n	Specify whether to connect a pull-up or pull-down resistor to the P47 to P40 pins.

PUIO	PDIO	Connection of a pull-up or pull-down resistor to the P47 to P40 pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

Remark n = 7 to 0

7.5.6 Port 5 Buffer function change register (DRCTLP5L, DRCTLP5H) <R>

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP5L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP52	PDIOP52	0	1	PUIOP51	PDIOP51	IOLP511	IOLP510	PUIOP50	PDIOP50	IOLP501	IOLP500	BASE+0248H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0000 0599H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP5H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP57	PDIOP57	0	1	0	0	0	0	0	0	0	0	0	0	0	0	BASE+024CH
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0000 9000H

Bit position	Bit name	Function
31 to 16	–	Reserved. (Be sure to write 0 to these bits. If read, 0 is returned.)
15, 14, 11, 10, 7, 6, 3, 2	PUIOP5n, PDIOP5n	Specify whether to connect a pull-up or pull-down resistor to the P57 and P52 to P50 pins.

PUIO	PDIO	Connection of a pull-up or pull-down resistor to the P57 and P52 to P50 pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

5, 4, 1, 0	IOLP5n1, IOLP5n0	Specify the driving capability of the P51 to P50 pins.<R>

IOL1	IOL0	Driving capability of P51 to P50 pins
0	1	6 mA (recommended)
1	1	12 mA
Other than above		Setting prohibited

Remark n = 7 to 0

7.5.7 Port 6 Buffer function change register (DRCTLP6L, DRCTLP6H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP6L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP63	PDIOP63	0	1	PUIOP62	PDIOP62	0	1	PUIOP61	PDIOP61	0	1	PUIOP60	PDIOP60	0	1	BASE+0250H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	0000 9999H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP6H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP67	PDIOP67	0	1	PUIOP66	PDIOP66	0	1	PUIOP65	PDIOP65	0	1	PUIOP64	PDIOP64	0	1	BASE+0254H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	0000 9999H

Bit position	Bit name	Function
31 to 16	–	Reserved. (Be sure to write 0 to these bits. If read, 0 is returned.)
15,14,11, 10,7,6,3.2	PUIOP6n, PDIOP6n	Specify whether to connect a pull-up or pull-down resistor to the P67 to P60 pins.

PUIO	PDIO	Connection of a pull-up or pull-down resistor to the P67 to P60 pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

Remark n = 7 to 0

7.5.8 Port 7 Buffer function change register (DRCTLP7L, DRCTLP7H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP7L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP73	PDIOP73	0	1	PUIOP72	PDIOP72	0	1	PUIOP71	PDIOP71	0	1	PUIOP70	PDIOP70	0	1	BASE+0258H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	0000 9999H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP7H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP77	PDIOP77	0	1	PUIOP76	PDIOP76	0	1	PUIOP75	PDIOP75	0	1	PUIOP74	PDIOP74	0	1	BASE+025CH
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	0000 9999H

Bit position	Bit name	Function
31 to 16	–	Reserved. (Be sure to write 0 to these bits. If read, 0 is returned.)
15,14,11, 10,7,6,3.2	PUIOP7n, PDIOP7n	Specify whether to connect a pull-up or pull-down resistor to the P77 to P70 pins.

PUIO	PDIO	Connection of a pull-up or pull-down resistor to the P77 to P70 pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

Remark n = 7 to 0

7.5.9 Real-time port 0 Buffer function change register (DRCTLRP0L, DRCTLRP0H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP0L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP03	PDIORP03	IOLRP031	IOLRP030	PUIORP02	PDIORP02	IOLRP021	IOLRP020	PUIORP01	PDIORP01	IOLRP011	IOLRP010	PUIORP00	PDIORP00	IOLRP001	IOLRP000	BASE+0260H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0000 9999H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP0H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP07	PDIORP07	IOLRP071	IOLRP070	PUIORP06	PDIORP06	IOLRP061	IOLRP060	PUIORP05	PDIORP05	IOLRP051	IOLRP050	PUIORP04	PDIORP04	IOLRP041	IOLRP040	BASE+0264H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0000 9999H

Bit position	Bit name	Function
31 to 16	–	Reserved. (Be sure to write 0 to these bits. If read, 0 is returned.)
15, 14, 11, 10, 7, 6, 3, 2	PUIORP0n, PDIORP0n	Specify whether to connect a pull-up or pull-down resistor to the RP07 to RP00 pins.
13, 12, 9, 8, 5, 4, 1, 0	IOLRP0n1, IOLRP0n0	Specify the driving capability of the RP07 to RP00 pins.

PUIO	PDIO	Connection of a pull-up or pull-down resistor to the RP07 to RP00 pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

IOL1	IOL0	Driving capability of RP07 to RP00 pins
0	1	6 mA (recommended)
1	1	12 mA
Other than above		Setting prohibited

Remark n = 7 to 0

7.5.10 Real-time port 1 buffer function change registers (DRCTLRP1L, DRCTLRP1H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP1L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP13	PDIORP13	IOLRP131	IOLRP130	PUIORP12	PDIORP12	IOLRP121	IOLRP120	PUIORP11	PDIORP11	IOLRP111	IOLRP110	PUIORP10	PDIORP10	IOLRP101	IOLRP100	BASE+0268H
																																	Initial value
																																	0000 9999H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP1H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP17	PDIORP17	IOLRP171	IOLRP170	PUIORP16	PDIORP16	IOLRP161	IOLRP160	PUIORP15	PDIORP15	IOLRP151	IOLRP150	PUIORP14	PDIORP14	IOLRP141	IOLRP140	BASE+026CH
																																	Initial value
																																	0000 9999H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Bit position	Bit name	Function
31 to 16	–	Reserved. (Be sure to write 0 to these bits. If read, 0 is returned.)
15,14,11, 10,7,6,3.2	PUIORP1n, PDIORP1n	Specify whether to connect a pull-up or pull-down resistor to the RP17 to RP10 pins.
13,12,9,8 5,4,1,0	IOLRP1n1, IOLRP1n0	Specify the driving capability of the RP17 to RP10 pins.

PUIO	PDIO	Connection of a pull-up or pull-down resistor to the RP17 to RP10 pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

IOL1	IOL0	Driving capability of RP17 to RP10 pins
0	1	6 mA (recommended)
1	1	12 mA
Other than above		Setting prohibited

Remark n = 7 to 0

7.5.11 Real-time port 2 Buffer function change register (DRCTLRP2L, DRCTLRP2H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP2L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP23	PDIORP23	IOLRP231	IOLRP230	PUIORP22	PDIORP22	IOLRP221	IOLRP220	PUIORP21	PDIORP21	IOLRP211	IOLRP210	PUIORP20	PDIORP20	IOLRP201	IOLRP200	BASE+0270H
																																	Initial value
																																	0000 5559H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP2H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP27	PDIORP27	IOLRP271	IOLRP270	PUIORP26	PDIORP26	IOLRP261	IOLRP260	PUIORP25	PDIORP25	IOLRP251	IOLRP250	PUIORP24	PDIORP24	IOLRP241	IOLRP240	BASE+0274H
																																	Initial value
																																	0000 5555H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Bit position	Bit name	Function
31 to 16	–	Reserved. (Be sure to write 0 to these bits. If read, 0 is returned.)
15,14,11, 10,7,6,3.2	PUIORP2n, PDIORP2n	Specify whether to connect a pull-up or pull-down resistor to the RP27 to RP20 pins.
13,12,9,8 5,4,1,0	IOLRP2n1, IOLRP2n0	Specify the driving capability of the RP27 to RP20 pins.

PUIO	PDIO	Connection of a pull-up or pull-down resistor to the RP27 to RP20 pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

IOL1	IOL0	Driving capability of RP27 to RP20 pins
0	1	6 mA (recommended)
1	1	12 mA
Other than above		Setting prohibited

Remark n = 7 to 0

7.5.12 Real-time port 3 Buffer function change register (DRCTLRP3L, DRCTLRP3H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP3L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP33	PDIORP33	IOLRP331	IOLRP330	PUIORP32	PDIORP32	IOLRP321	IOLRP320	PUIORP31	PDIORP31	IOLRP311	IOLRP310	PUIORP30	PDIORP30	IOLRP301	IOLRP300	BASE+0278H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0000 9999H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP3H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP37	PDIORP37	IOLRP371	IOLRP370	PUIORP36	PDIORP36	IOLRP361	IOLRP360	PUIORP35	PDIORP35	IOLRP351	IOLRP350	PUIORP34	PDIORP34	IOLRP341	IOLRP340	BASE+027CH
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0000 9999H

Bit position	Bit name	Function
31 to 16	–	Reserved. (Be sure to write 0 to these bits. If read, 0 is returned.)
15,14,11, 10,7,6,3.2	PUIORP3n, PDIORP3n	Specify whether to connect a pull-up or pull-down resistor to the RP37 to RP30 pins.
13,12,9,8 5,4,1,0	IOLRP3n1, IOLRP3n0	Specify the driving capability of the RP37 to RP30 pins.

PUIO	PDIO	Connection of a pull-up or pull-down resistor to the RP37 to RP30 pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

IOL1	IOL0	Driving capability of RP37 to RP30 pins
0	1	6 mA (recommended)
1	1	12 mA
Other than above		Setting prohibited

Remark n = 7 to 0

7.6 Operation of port functions

The port operation differs depending on the I/O mode setting, as shown below.

7.6.1 Reading and writing via I/O ports

(1) In output mode

If a value is written to port register n (Pn or RPn), the value is written to that port's output latch (Pn or RPn). The value of the output latch is output from the pin.

The value written to the output latch is held until another value is written.

The value of the output latch (Pn or RPn) can be read by reading port register n (Pn or RPn).

To directly read the pin level, read port pin input register n (PINn or RPINn).

(2) In input mode

If a value is written to port register n (Pn or RPn), the value is written to that port's output latch (Pn or RPn). However, the pin status does not change because the output buffer is off.

The value written to the output latch is held until another value is written.

To read the input level, read port pin input register n (PINn or RPINn).

7.6.2 Alternate function pin output status in control mode

The port pin level can be read directly by reading port pin input register n (PINn or RPINn), regardless of the settings in the PMCn, PMn, PFCn, and PFCEn registers.

7.7 Trigger-synchronous ports (RP00 to RP37)

The status of the 32-bit port pins RP00 to RP37 is updated in synchronization with an interrupt from an on-chip peripheral function.

Use the RPTRGMD register to specify whether to set a port to trigger-synchronous port control mode in 1-bit units. To select the trigger, use the RPTFR0 to RPTFR3 registers.

For details, see R-IN32M3 User's Manual - Peripheral Functions.

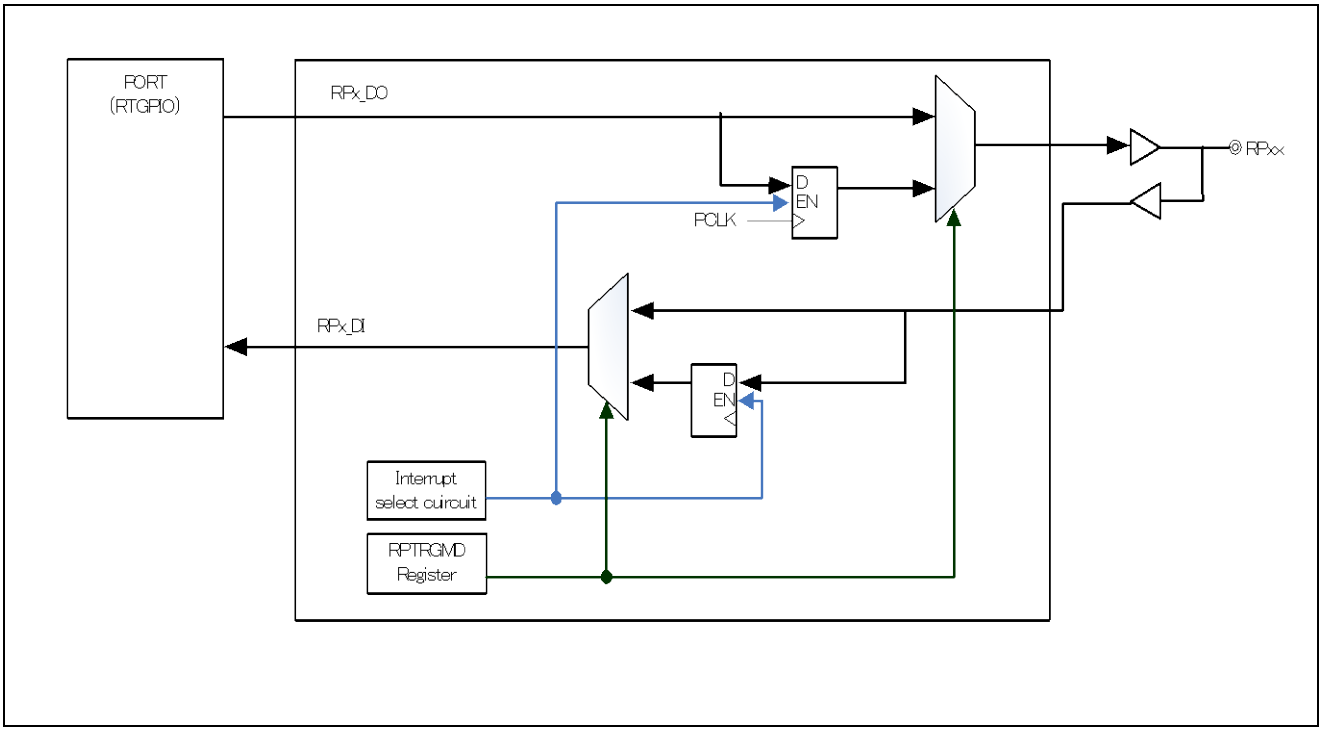


Figure 7.18 Configuration of Trigger-Synchronous Ports

8. Electrical Specifications

Please refer to R-IN32M3 series datasheet for the Electrical Specifications.

REVISION HISTORY	R-IN32M3-CL User's Manual

Rev.	Date	Description	
		Page	Summary
1.00 (Preliminary)	2013.2.8	-	First edition issued
1.00	Apr 03,2013	overall	Modification of English expressions
		overall	Change the description of "CC-Link IE Field" "CC-Link IE Field Slave" → "CC-Link IE Field (Intelligent device station)"
		overall	Change the description of "CC-Link" "CC-Link (Slave)" → "CC-Link (Remote device station)"
		1	Modification of the contents of ***1.1 Introduction***
		2	Modification of the status of ETH_MDC during the reset of ***2.1.1 Ethernet Signals*** Modification of the contents of Note of ***2.1.1 Ethernet Signals***
		3	Standby mode deletion
		8	Modification of the status of BUSCLK during the reset of ***2.1.2 External Memory Interface Signals*** Addition of synchronous burst access MEMC information of ***2.1.2 External Memory Interface Signals***
		9	Modification of the status of HD0-HD15, HBCYSTZ during the reset of ***2.1.3 External MCU Interface Signals***
		20	Modification of PONRZ function of ***2.1.16 System Signals*** Addition the signals of HOTRESETZ, VDDQ_MII, CLKOUT25M0, CLKOUT25M1 of ***2.1.16 System Signals***
		22	Modification of the contents of Note1 and Note2 of ***2.2Port status***
1.01	Dec 09 2013	overall	Modification of the supported station of CC-Link
2.00	Feb 07,2014	4	Modification of block diagram of **1.3 INTERNAL BLOCK DIAGRAM**
		6-21	Addition the status after reset timing of ***2.1 Signals by function***
		17	Addition explanation of Function of ***2.1.13 CC-Link IE Field Signals***
		19	Add ***CCM_CLK80M*** pins to list of ***2.1.15 CC-Link Signals (Remote device station)***
		21	Modification of Boot mode select of ***2.1.18 Operation mode Setting Signals***
		22	Addition of Synchronous burst MEMC of ***2.2 Port status***
		25	Addition of the signals of CLKOUT25M0/CLKOUT25M1 of ***2.5.3 System Signals***
		27-28	Addition of a resistor value of Pull up/down of ***2.3.5 Port Signals*** Modification of a description of the drive current of P30/P31/P52/P61-P64 of ***2.3.5 Port Signals***
		28	Modification of title name of ***2.5.8 CC-Link Signal (Intelligent device station, Remote device station)***
		37	Addition of the contents of Note of INTCCSRFSTB register of ***4.2 Inerruput list***
		40	Addition the register of ***6.1.1 CC-Link IE Field (Intelligent device station) clock gate register***

Rev.	Date	Description	
		Page	Summary
2.00	Feb 07,2014	41	Addition the register of ***6.1.2 CC-Link IE Field (Intelligent device station) wait delay register***
		42	Modification of Address of ***6.1.4 CC-Link IE Field (Intelligent device station) bus bridge control register (CIESMC)***
		57	Modification of initial value of PM0W, PM4W, and PRM0W registers of ***7.3.2 Port mode registers (PM, RPM)***
2.01	Apr 18,2014	overall	Modification of ***CC-Link Signals (Remote device station)***
		17	Addition of the contents of Note of **2.1.13 CC-Link IE Field Signals (Intelligent device station)**
		28	Modification of pin setting of **2.5.7CC-Link IE Field Signal (Intelligent device station)**
		71	Addition of the signals of CCI_WAITEDGEH / CCI_WRLENH of **7.4 Available combinations of alternate functions**
2.02	Dec 25, 2014	3	Change status for Intelligent device station for CC-Link in ***1.3 Overview***
		80	Remove IOLP521, IOLP520 bit at ***7.5.6 Port 5 buffer function change registers (DRCTLP5L, DRCTLP5H)*** (because driving capability of P52 is fixed to 6mA.)

[Memo]

R-IN32M3 Series User's Manual
R-IN32M3-CL

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